NEX-SRIO2

Serial RapidIO Gen2 Protocol Analyzer
Product Manual

for use with the TLA6404
Rev. 0.2

Warranty Terms and License Agreement

For warranty terms, refer to the Terms and Conditions of Sale document that was included in the product shipment. The Software License Agreement is displayed during installation. A hardcopy of that agreement may be obtained from Nexus Technology.

All Nexus Technology products to which this manual refers are subject to the Terms and Conditions of Sale document and the Software License Agreement, as appropriate.

Compliance with WEEE and RoHS Directives

This product is subject to European Union regulations on Waste Electrical and Electronics Equipment. Return to Nexus Technology for recycle at end of life. Costs associated with the return to Nexus Technology are the responsibility of the sender.

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1.0 Overview

1.1 Contact Information / Support

1.1.1 About Nexus Technology, Inc.

Established in 1991, Nexus Technology, Inc. is dedicated to developing, marketing, and supporting bus analysis applications.

We can be reached at:

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78 Northeastern Blvd. Unit 2

Nashua, NH 03062

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Fax: 877-595.8118

1.1.2 Support Contact Information

Product Support support@nexustechnology.com

Normal business hours are 9AM to 5PM EST/EDT

1.2 Conventions Used in This Manual

SRIO: Serial RapidIO

SRIO Gen2: Serial RapidIO Specification 2.1

SRIO Gen1: Serial RapidIO Specification 1.3

Lane: A unidirectional, serial, differential pair

1x Mode: 1x LP-Serial physical layer definition (1 lane)

2x Mode: 2x LP-Serial physical layer definition (2 lanes)

4x Mode: 4x LP-Serial physical layer definition (4 lanes)

Tx: Transmit or transmitter

Rx: Receive or receiver

Datapath: A Tx or Rx stream of data (1x mode or 4x mode)

TLA: A Tektronix Logic Analyzer system

SUT: The System Under Test

1.3 Product Description

This product includes all the hardware and software necessary to analyze an SRIO SUT and interface a Tektronix logic analyzer to one or more serial probes. The serial probes (separate product manual) provide an interface between this product and the SUT. This product enables logic analyzer acquisition of combinations of SRIO Gen2 or Gen1, 4x/2x/1x datapath(s) at speeds of 6.25-1, 5.00-1, 3.125-, 2.50-, or 1.25-Gbps (depending on options purchased). SUT must meet minimum eye sizes for reliable acquisition. This product also enables pattern injection on to a SRIO Gen2 or Gen1 4x/2x/1x datapath at speeds of 6.25-1, 5.00-1, 3.125-, 2.50-, or 1.25Gbps SUT, if that option has been purchased.

1.4 Included With this Product

Equipment/Software	Description	Included	Quantity	Manual
NEX-SRIO2	SRIO2 Protocol Analyzer	Yes	1	This document.
AC Power Cable		Yes	1	This document.
Keyboard		Yes	1	This document.
Mouse		Yes	1	This document.
Software Media	Software installation	Yes	1	This document.
TLA Probe Labels		Yes	6	This document.

Table 1 - Included with this Product

1.4.1 Software

1.4.1.1 SRIO2 Protocol Analyzer Setup

Software is provided pre-installed on the NEX-SRIO2 unit to configure the protocol analyzer for proper analysis, pattern injection (if purchased) and presentation to the Tektronix logic analyzer.

1.4.1.2 Logic Analyzer Setup

A support package must be installed on the TLA to configure the system to properly acquire and decode the SRIO traffic. This setup provides easy access to the SRIO raw data or the decoded data. Software is also provided to easily apply advanced triggering and filtering of the SRIO traffic.

1.5 SRIO Target Requirements

1.5.1 SRIO Eye Size Requirements

The eye size required at the serial probe point is a perfect diamond shaped, stable eye based on the values in *Table 2*. Capture accuracy may be affected if this minimum eye size is not met. The serial probes have manuals separate from this document.

Minimum Eye Height (Single-ended)	*30mV*
Minimum Eye Width @ 6.25-Gbps	90ps
Minimum Eye Width @ 5.00-Gbps	110ps
Minimum Eye Width @ 3.125-Gbps	180ps
Minimum Eye Width @ 2.50-Gbps	220ps
Minimum Eye Width @ 1.25-Gbps	430ps

Table 2 – Minimum Eye Size Requirements

2.0 SRIO Analyzer Chassis

The key components of the front and back of the chassis can be found in *Figure 1* and *Figure 3*.

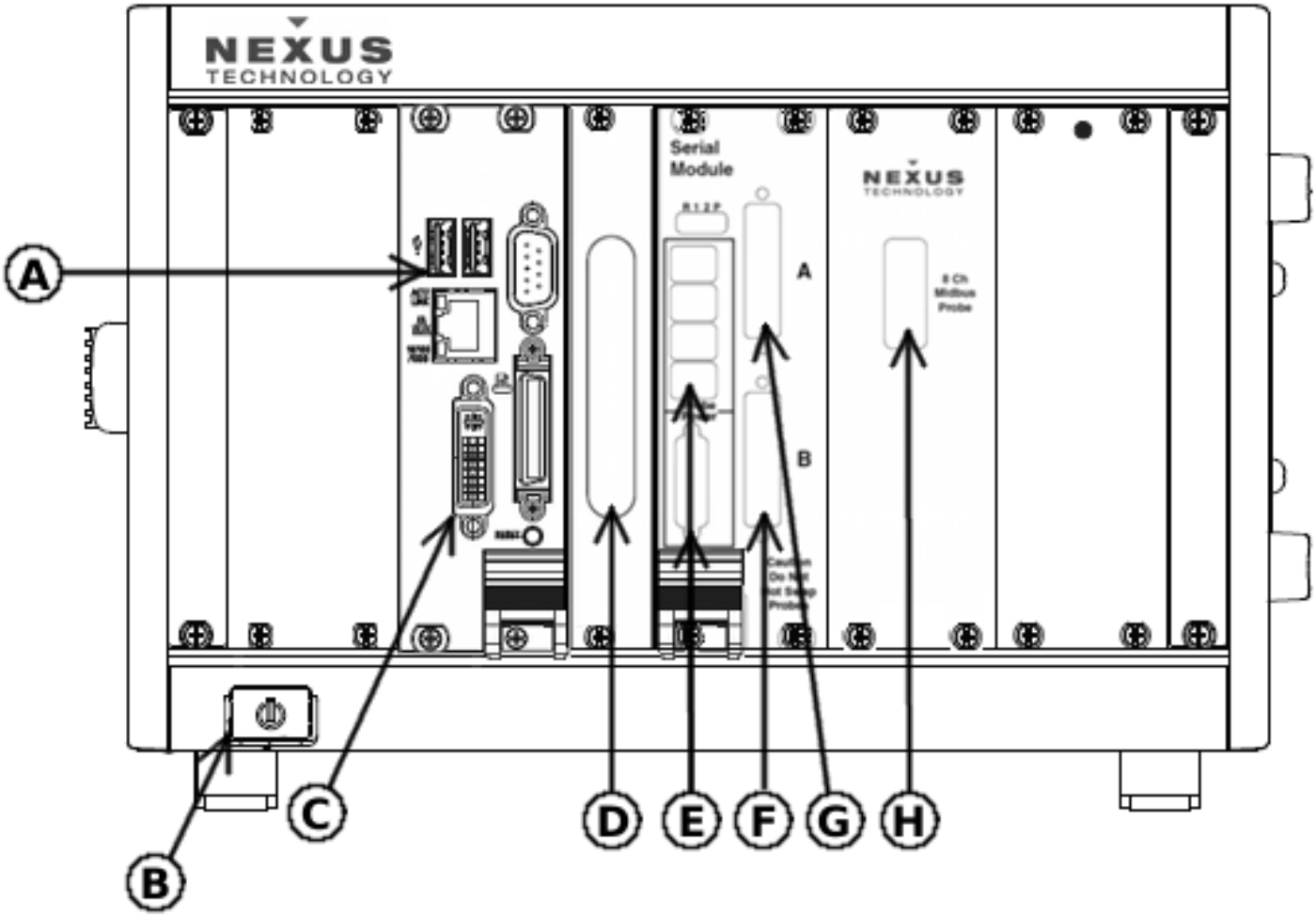

Figure 1 - Front View of Chassis

A	USB for keyboard and mouse
B	System Power Switch
C	Monitor
D	Exit port for logic analyzer probes
E	Serial probe power connections
F	Serial probe data connections for Datapath B
G	Serial probe data connections for Datapath A
H	8-channel mid-bus probe connection for self-test

Figure 2 - Key Components of Front Chassis

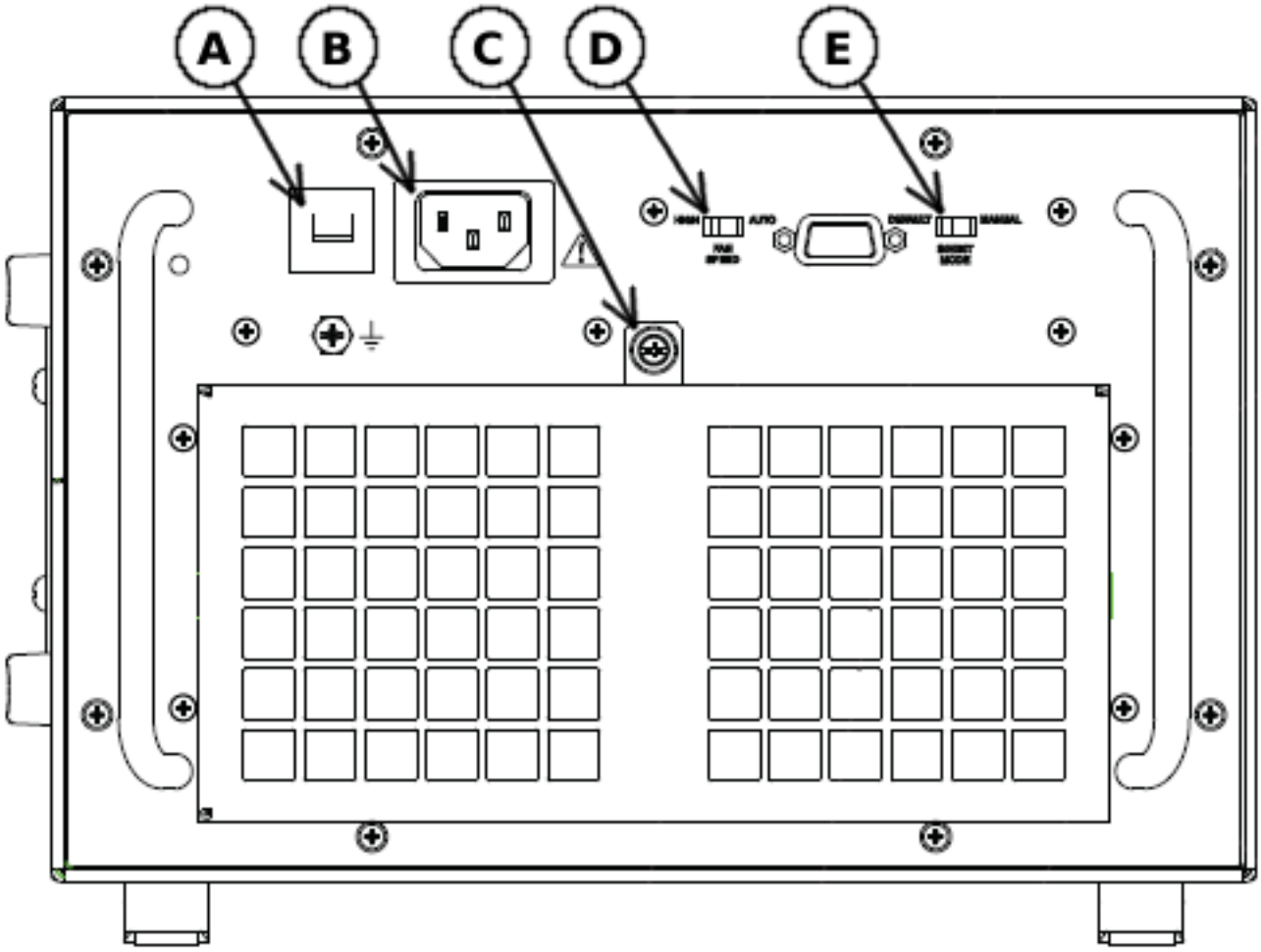

Figure 3 - Back View of Chassis

A	Circuit Breaker
B	AC Input
C	Air filter retainer screw
D	Fan speed (should be left at Auto)
E	Inhibit mode (should be left at Default)

Figure 4 - Key Components of Back Chassis

3.0 Overview of Logic Analyzer Acquisition

3.1 Acquisition

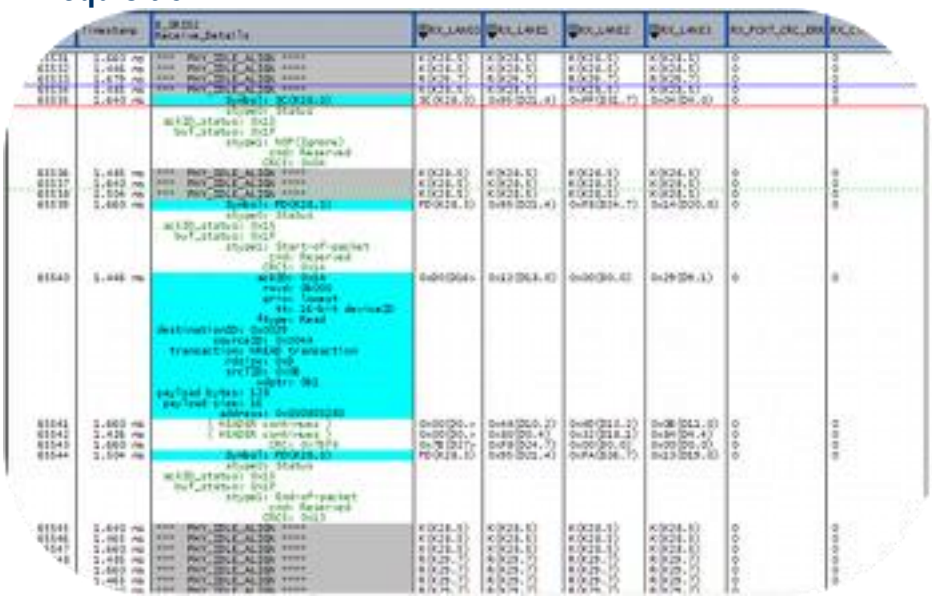

Figure 5 - Example SRIO Data

The Tektronix Logic Analyzer (TLA) provides access to the raw and decoded data from the SRIO analyzer. The TLA is a powerful, general purpose, analyzer with many setup options and advanced features. The SRIO analyzer includes support setup software which automatically configures the TLA. This allows the user to be up, running, and acquiring data very quickly.

The SRIO analyzer sends all SRIO traffic to the TLA for storage. No data is ever filtered from the acquisition unless a filter is explicitly enabled.

3.2 4x, 2x, and 1x Data Presentation to the Logic Analyzer

All SRIO control symbols and packets are aligned in the logic analyzer for easy analysis, filtering, and triggering.

In 4x mode, 4 lanes of traffic are utilized on the SUT. These are referred to as Lane0, Lane1, Lane2, and Lane3. The SRIO specification requires all data be word aligned to 32-bit2 boundaries beginning with Lane0 data and ending with Lane3 data. This data is presented to the logic analyzer without modification.

In 2x mode, 2 lanes of traffic are utilized on the SUT. These are referred to as Lane0 and Lane1. This data is stacked across all four lanes to the logic analyzer such that valid data will appear on all four lanes: Lane0, Lane1, Lane2, and Lane3. The data is also word aligned such that all control symbols and packets begin on Lane0. The word alignment will require injection of PAD characters into the data stream of Lane1, Lane2, or Lane3. Any PAD characters injected into the data stream do not affect the decoding or analysis of the acquired data.

In 1x mode, 1 lane of traffic is utilized on the SUT. This lane is referred to as Lane0. The data is stacked across all four lanes to the logic analyzer such that valid data will appear on all four lanes: Lane0, Lane1, Lane2, and Lane3. The data is also word aligned such that all control symbols and packets begin on Lane0. The word alignment will require injection of PAD characters into the data stream of Lane1, Lane2, or Lane3. Any PAD characters injected into the data stream do not affect the decoding or analysis of the acquired data.

4.0 Logic Analyzer Setup

4.1 First Time Setup

This product comes with 8 labels. Two or four of these labels should be applied to the logic analyzer connections, replacing the generic labels of 'A', 'B', etc. The labels are applied differently depending on the logic analyzer configuration you have. Please see *Table 3* below.

SRIO2 Analyzer Generic Label	2- TLAxx2 Replacement	2- TLA7Ax4 Modules	TLAxx4 or TLAxx3 Replacement
A	A- C3/C2/A3/A2	A- A3/A2/D3/D2	A- E3/E2/E1/E0
B	A- A1/A0/D1/D0	A- A1/A0/D1/D0	A- A1/A0/D1/D0
C	B- A1/A0/D1/D0	B- A3/A2/D3/D2	B- A3/A2/D3/D2
D	B- C3/C2/A3/A2	B- A1/A0/D1/D0	B- C3/C2/C1/C0

Table 3 - Probe Labels

4.2 Connecting to the Logic Analyzer

The SRIO analyzer has two or four connections to the logic analyzer module, depending on configuration. If this is the first use of the product, please see *First Time Setup*. If not, the SRIO analyzer should be connected to the Tektronix logic analyzer following the labels on the SRIO analyzer connectors. If using two TLA7Ax4 modules, the 'A' and 'B' connections should NOT be split between modules. **It should be noted which module uses the 'A' connections and which module uses the 'B' connections so that the correct support package can be loaded for each module.**

4.3 Installing the Required Software

All software included with this product is provided on physical media, such as a CD. The logic analyzer configuration files can be installed by following the directions below.

4.3.1 Installing Logic Analyzer Support Software

To install the logic analyzer configuration software, navigate to the support_software folder on the provided media. From this folder run the appropriate installer. The selected software will then be installed on the computer. The correct software can be found in *Table 4*.

TLA Configuration Software	Description
B_SRIO2	Choose this if using one TLA7BB4
B_SRIO2_T102 and B_SRIO2_R102	Choose this if using one or two TLA7BB3. Note that 'T' corresponds to the transmit or Datapath 'A' and 'R' corresponds to the receive or Datapath 'B' data.
B_SRIO2_T68 and B_SRIO2_R68	Choose this if using one or two TLA7BB2. Note that 'T' corresponds to the transmit or Datapath 'A' and 'R' corresponds to the receive or Datapath 'B' data.
SRIO2_272	Choose this if using two, merged TLA7Ax4 modules
SRIO2_102	Choose this if using any of the following: TLA6xx3, TLA6xx4, TLA7Ax3, or TLA7Ax4
SRIO2_68	Choose this if using either a TLA6xx2 or a TLA7Ax2

Table 4 - Support Versions

4.3.2 Installing SRIO Triggering / Filtering Tool

To install the SRIO Triggering / Filtering tool, navigate to the pc_software folder on the provided media. From this folder run the MSI installer and follow the onscreen instructions. It will be necessary to restart the Tektronix Logic Analyzer Application after installation.

To remove any of the software, close the Logic Analyzer Software Application, run Windows Add/Remove Programs, select, and remove the software as named in the Add/Remove Programs list.

4.4 Loading the Required Software in the TLA

The appropriate support package can be loaded into the TLA Application software by following the steps below.

1. Press F9.
2. If using two modules, note which datapath is connected to which module. Datapath 'A' data corresponds to transmit data and require the correct transmit support package (B_SRIO2_T68) and Datapath 'B' data corresponds to receive data and requires the correct receive support package (B_SRIO2_R68).
3. In the System Window that appears, select the module(s) that the SRIO analyzer is connected to. The module will appear highlighted when selected.
4. From the *File* menu, select *Load Support Package…*
5. Select the appropriate support package name (see *Table 4*) and click *OK*.

If the SRIO Triggering / Filtering Tool has been installed, it can be loaded inside the TLA Application software by going to the *Tools* menu and selecting *NEX-SRIO-TRIGGERS*.

The TLA6404 uses a different probe than the BB module. The default threshold setting provided in the support package needs to be adjusted to 600mV. To do this, click *Synchronous* and in the *Global Threshold*, change 1.6V to 600 mV.

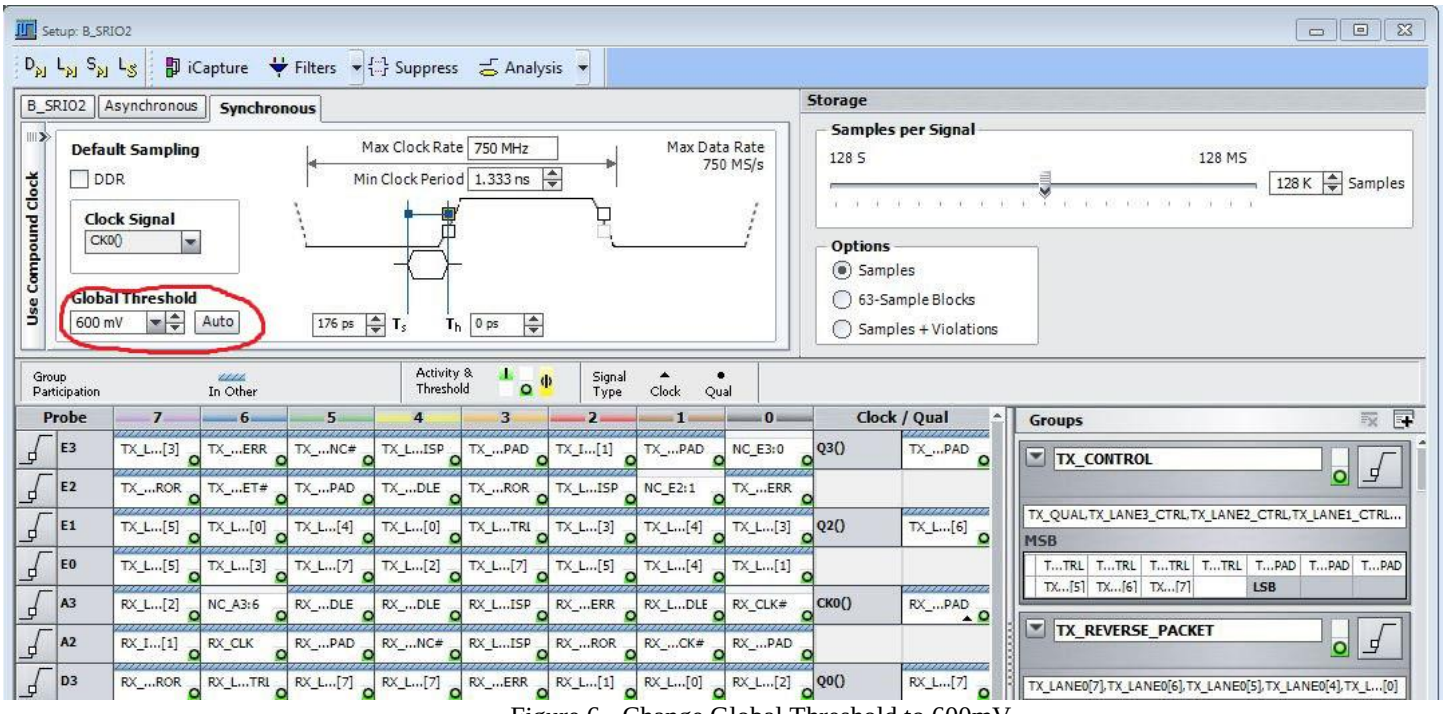

Figure 6 - Change Global Threshold to 600mV

The Tektronix logic analyzer is now setup up and ready to start acquiring data.

4.5 Support (disassembly) Software

Once the correct support software is loaded on the correct module(s), the TLA will be configured to display the SRIO protocol detail for the acquired data in a listing window. To view the SRIO information, simply add a listing window for the correct module and support package. *Figure 7* shows an example of selecting a module that has a support (B_SRIO2) loaded. The resulting listing window is shown in *Figure 8*.

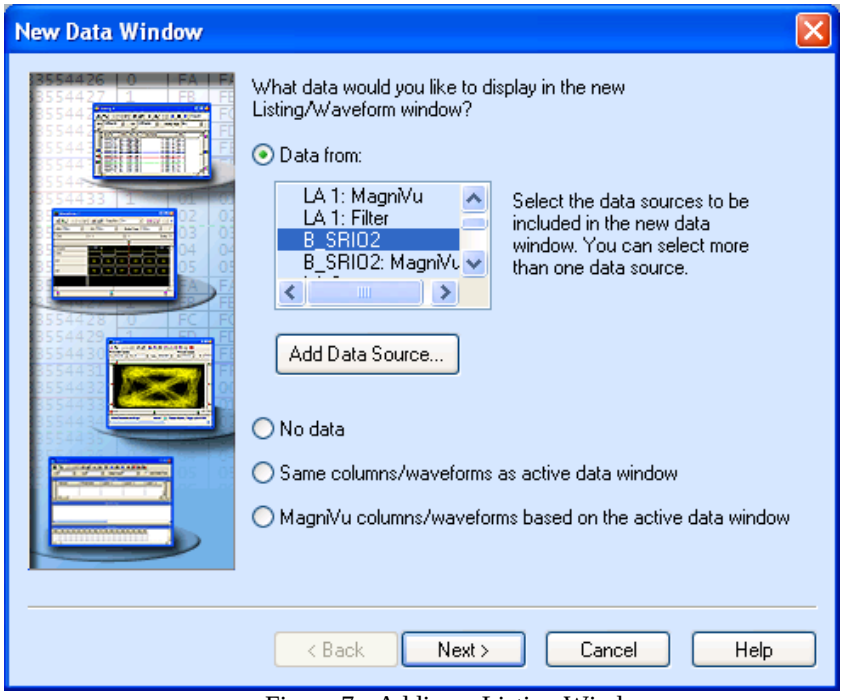

Figure 7 - Adding a Listing Window

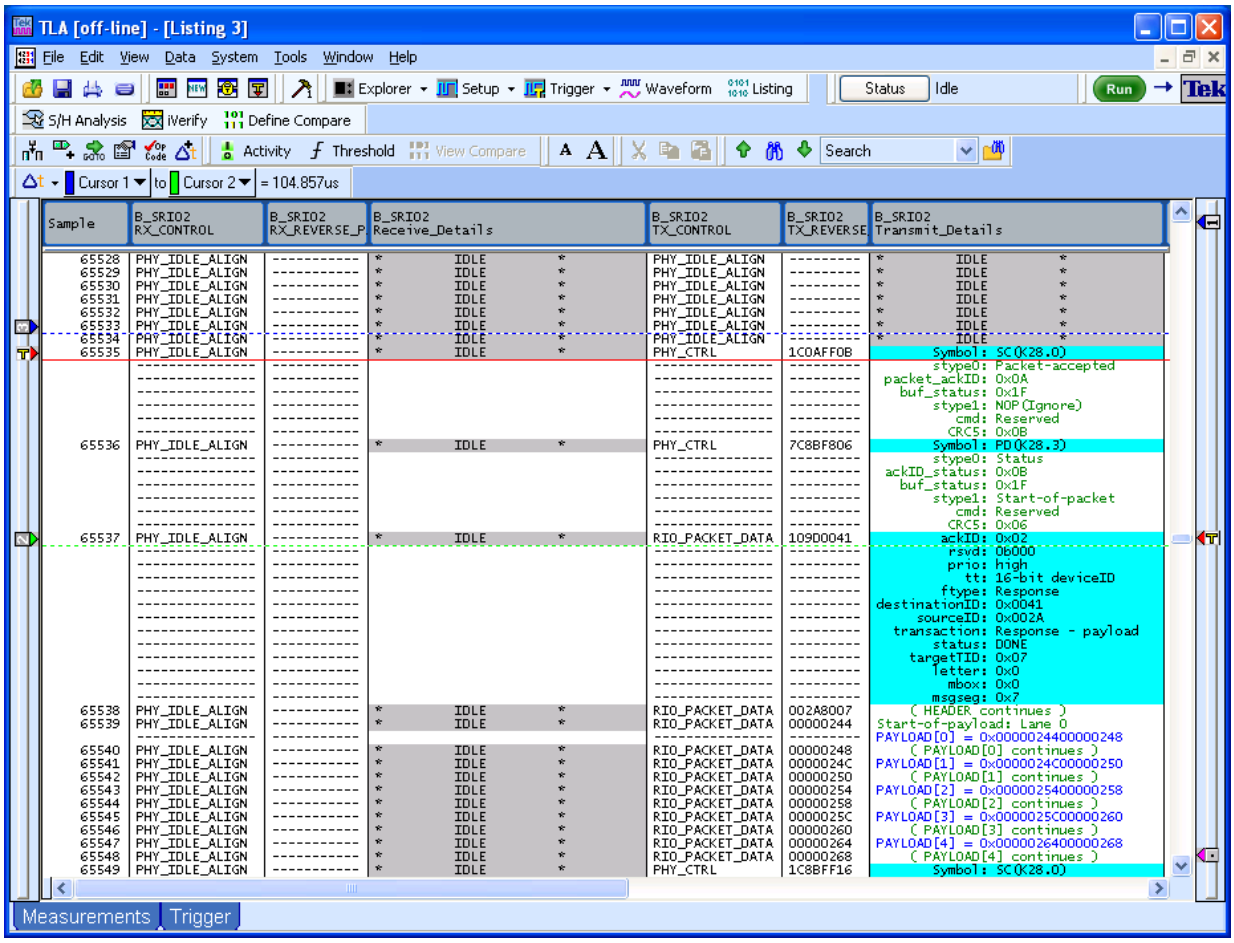

Figure 8 - SRIO Listing Window

There are some options on how the SRIO information is displayed. These may be accessed by clicking the right mouse button over a column heading. This brings up the Properties dialog, where the controls are located under the Disassembly tab (see *Figure 9*).

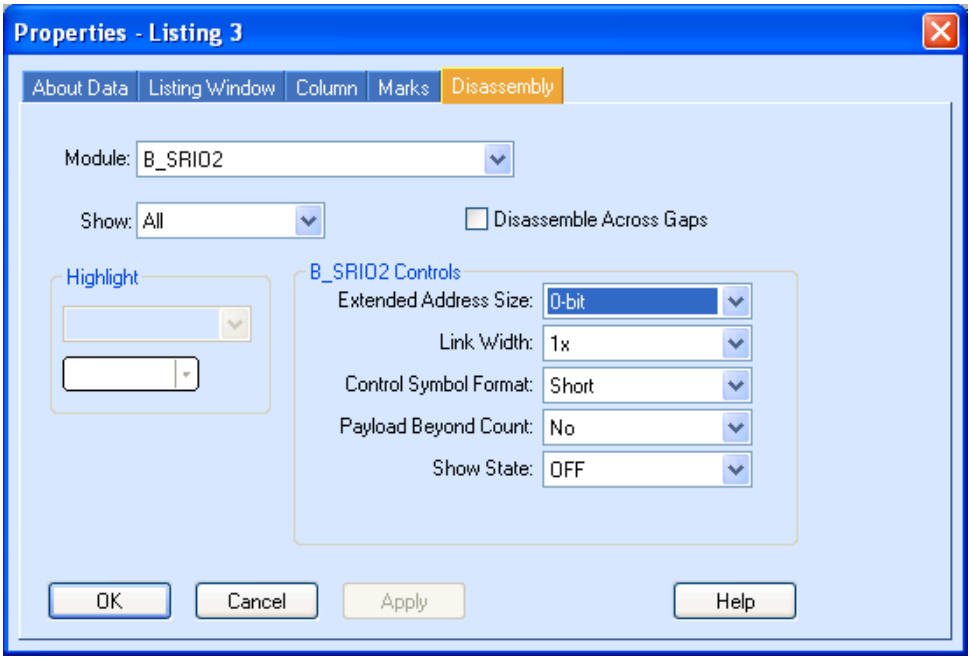

Figure 9 - Disassembly Properties

4.6 SRIO2 Configuration Software

The SRIO2 Protocol Analyzer unit comes with the pre-processor card and configuration software pre-installed. When the configuration software (Nexus Srio2) is started, the main form is displayed ().

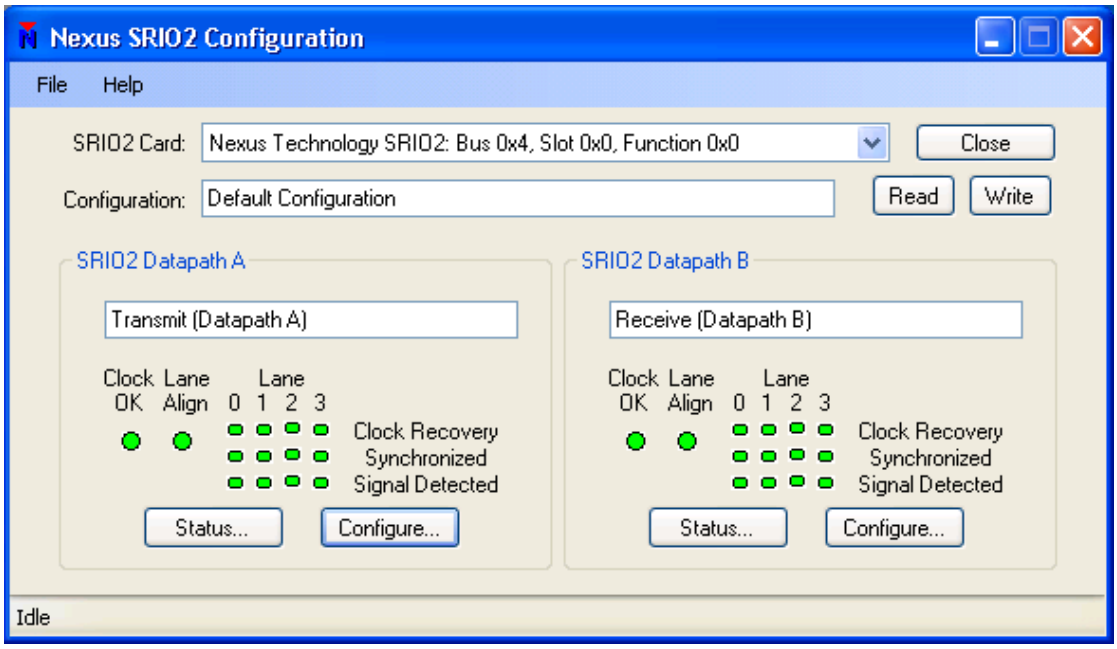

Figure 10 - Nexus Srio2 Main Form

The *File* menu (*Figure 111*) provides the ability to:

- Load and Save Configurations
- Clear the log file
- Turn on/off automatic update of status information
- Output more detailed logging (for Nexus debug assistance)

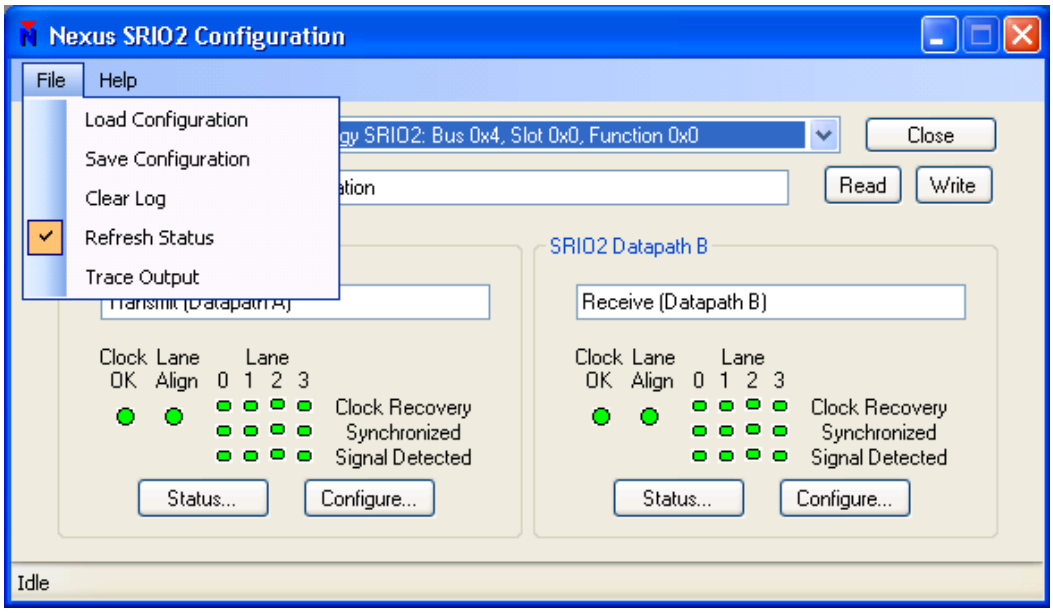

Figure 11 - File Menu Options

A Configuration is a complete set of setup information for the pre-processor (except pattern data). When started for the first time, a default configuration is loaded into the application. Subsequent start-up will load the last configuration information from the last time the application was run.
The automatic update will periodically refresh the status lights indicating the state of the pre-processor synchronization to the SRIO target.

The *About* menu provides the About option, which will display version information ().

Figure 12 - About Dialog

To control the pre-processor, first the card must be selected in the drop-down list (*Figure 133*).

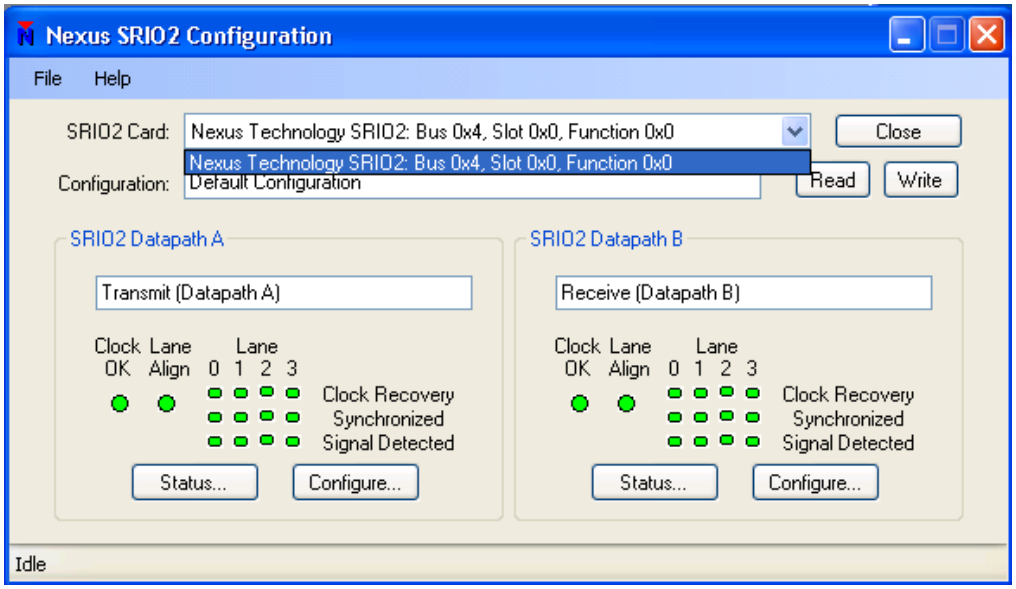

Figure 13 - SRIO Pre-processor Selection

Once the card is selected, the *Open* button is clicked. Note that the button changes to *Open* when the card is not connected and *Close* when it is connected.
When the application initially connects to the card, if the card has not been configured, the current configuration is loaded onto the card. If the card is already configured, the configuration information is loaded from the card and displayed for review and adjustment. Once the application is communicating with the card, the entire configuration may be read or written by the *Read* and *Write* buttons.
Detailed status may be obtained by clicking the appropriate *Status…* button. This displays the configuration dialog for the matching Datapath (*Figure 14*).

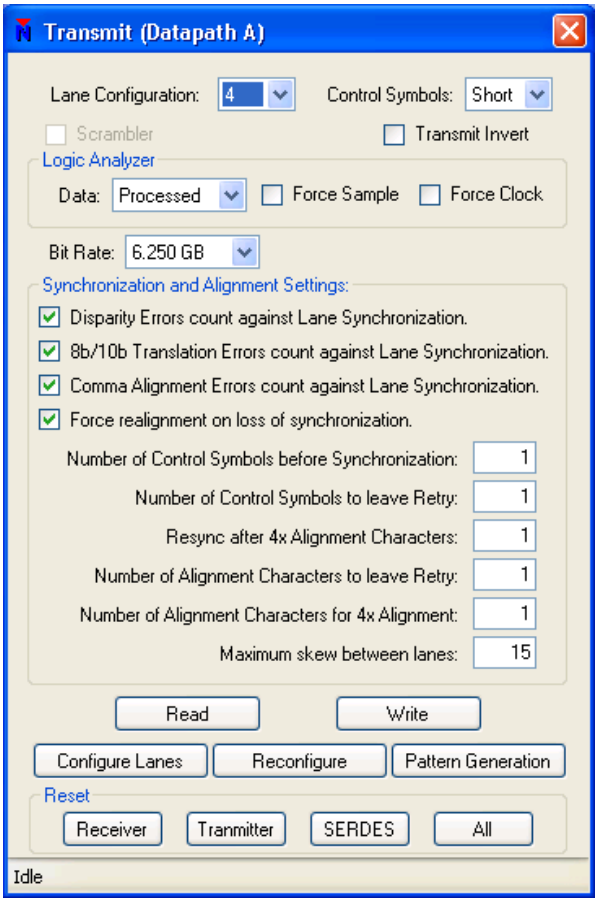

Figure 14 - Datapath Configuration

This dialog allows the configuration of:

- Active Lanes (1x, 2x, 4x)
- Control Symbol length (Short or Long)
- Logic Analyzer data
- Bit Rate
- Synchronization and Alignment Settings

Additionally, this dialog provides the ability to read and write the values, reset one or both datapaths (if available) and the entire SRIO connection. It also provides access to Configuring the lanes, reconfiguration and pattern generator (if purchased).
The *Configure Lanes* button will display the Lane Configuration dialog (*Figure 15*). This allows control of the lane arrangement, including the crossbar where the lane order can be re-arranged. Disparity errors may also be injected from this dialog.

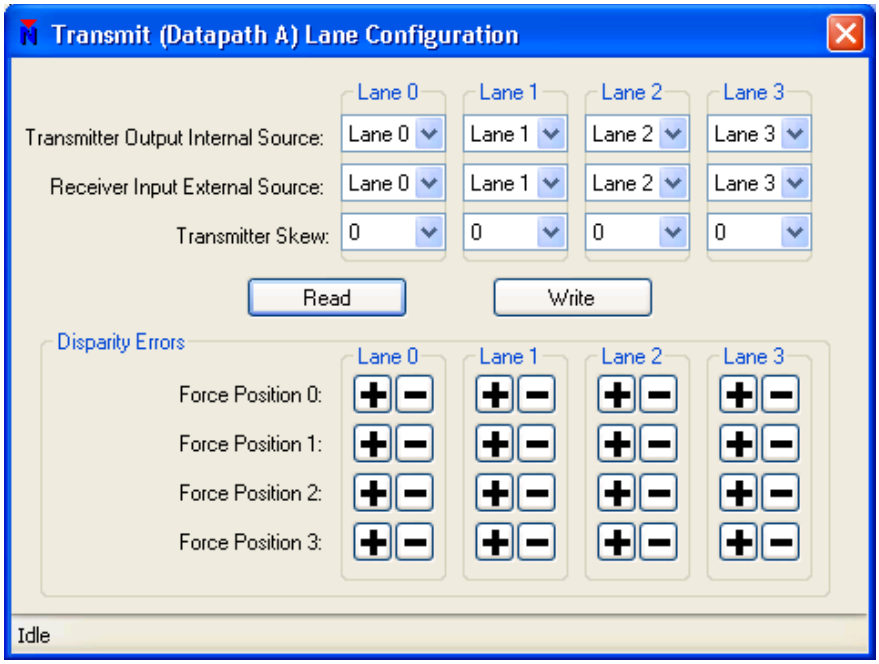

Figure 15 - Lane Arrangement and Error Injection

The *Reconfigure* button will display the individual lane configuration information (*Figure 16*). This allows tuning of the individual lane to account for target differences.

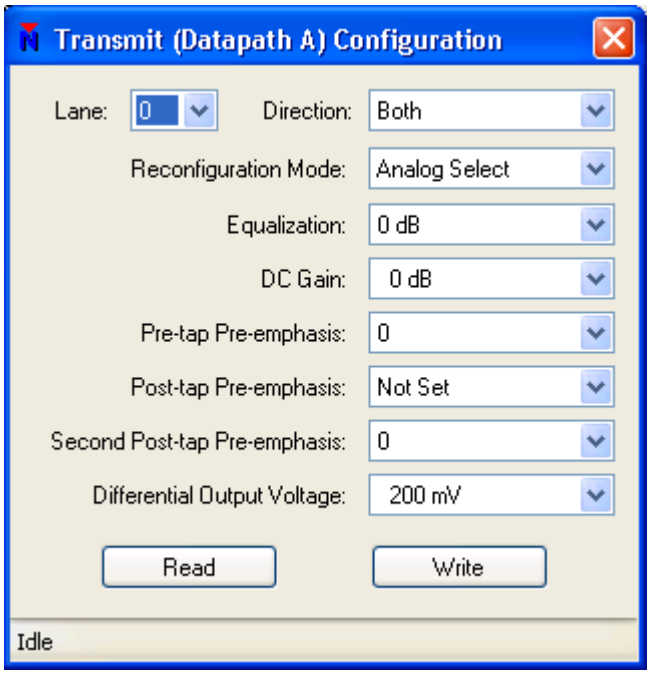

Figure 16 – Individual Lane Configuration

The *Pattern Generation* button will display the Pattern Generator dialog, if purchased (*Figure 17*). Note that the Pattern Generator dialog is modeless and can remain up while the other dialogs are used.

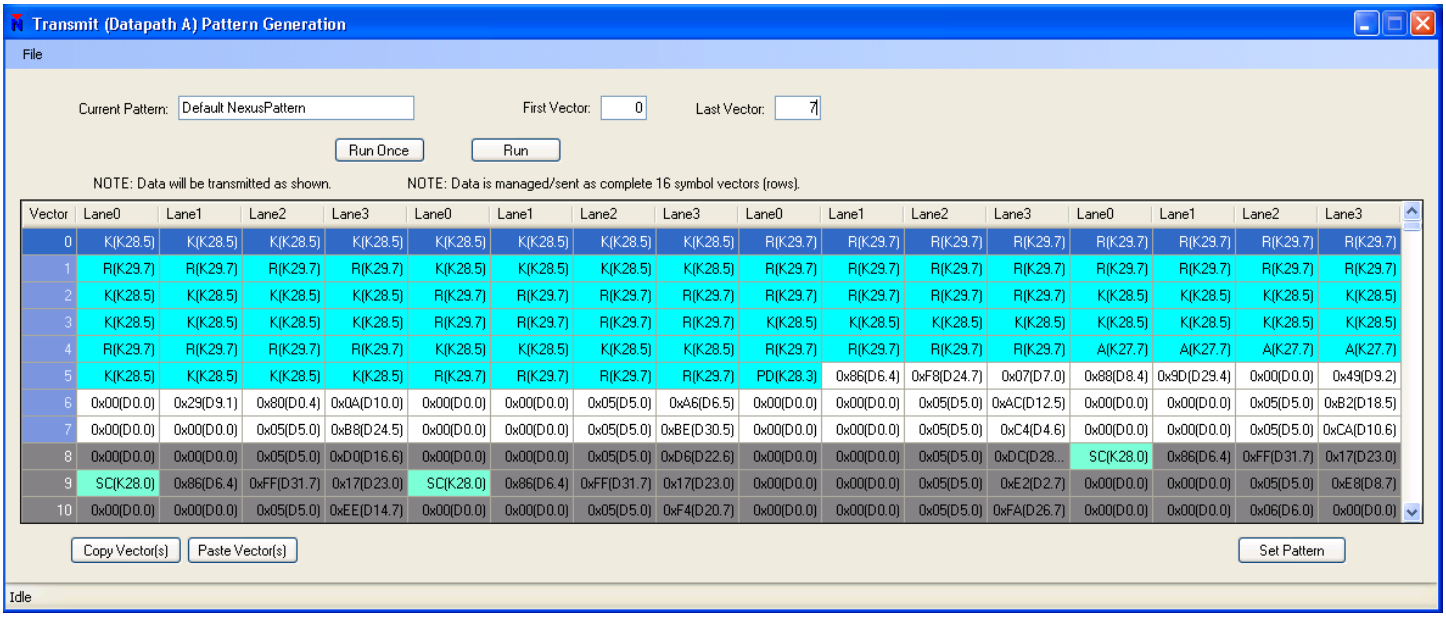

Figure 17 - Pattern Generation

This dialog supports:

- Load, Save and Import Patterns (*File* Menu)
- Edit Pattern
- Set pattern in card (*Set Pattern*)
- Control *First Vector* and *Last Vector* to output
- *Run Once*
- *Run* Continuously

Although data may be entered directly into the cells of the editor, there are a few features that will make editing a good bit easier.

- Double-clicking on a cell will bring up the 8b/10b character selection dialog, which allows selection of a Control Symbol (*Figure 18*) or a Data Symbol (*Figure 19*)
- One or more contiguous (shift-click) or non-contiguous (alt-click) vectors may be selected (*Figure 2020*) and copied, then pasted (*Figure 211*). By selecting a destination vector which is the first vector where the data copy should be placed, the copied data will be written to the appropriate vectors. Note that the data shape is preserved during the copy; meaning that, for example, as vector 2 was not selected (leaving a gap in the data), the data in vector 22 was not altered. In other words, vector offset is preserved in dis-contiguous data copy operations.

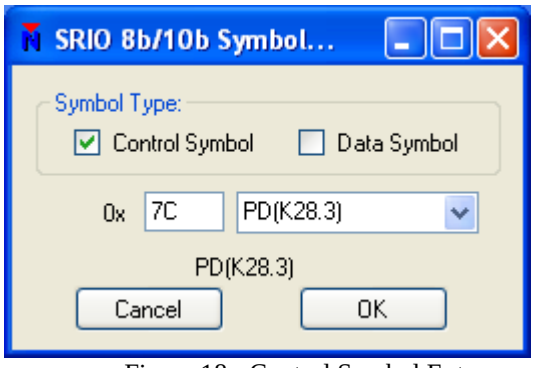

Figure 18 - Control Symbol Entry

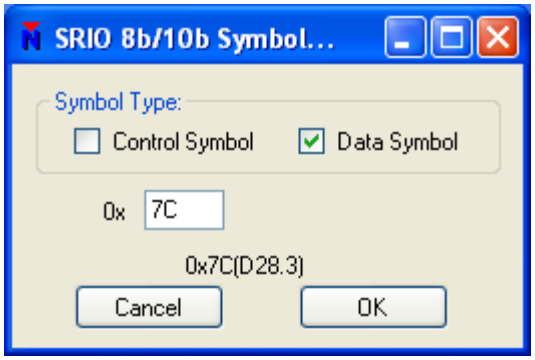

Figure 19 - Data Symbol Entry

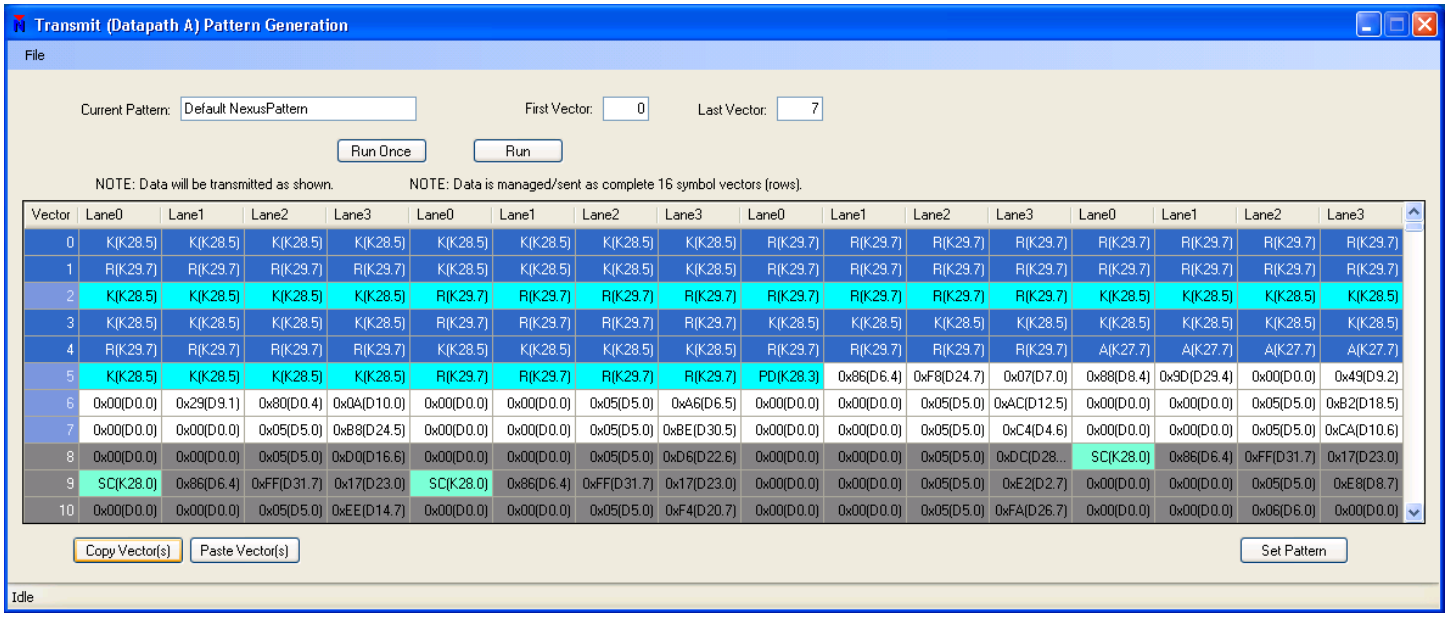

Figure 20 - Multi-vector Selection

Figure 21 - Multi-vector Paste

Data that has been correctly exported from the TLA or provided as text data may be imported, also. See *Figure 222* for format example. White space is not significant. Any element containing "LANE" is ignored and the data is imported in the order it was originally received (Lane0, Lane1, Lane2, Lane3, then to next line) and allocated into vectors in the same order. The resulting data after import is shown in *Figure 23*.

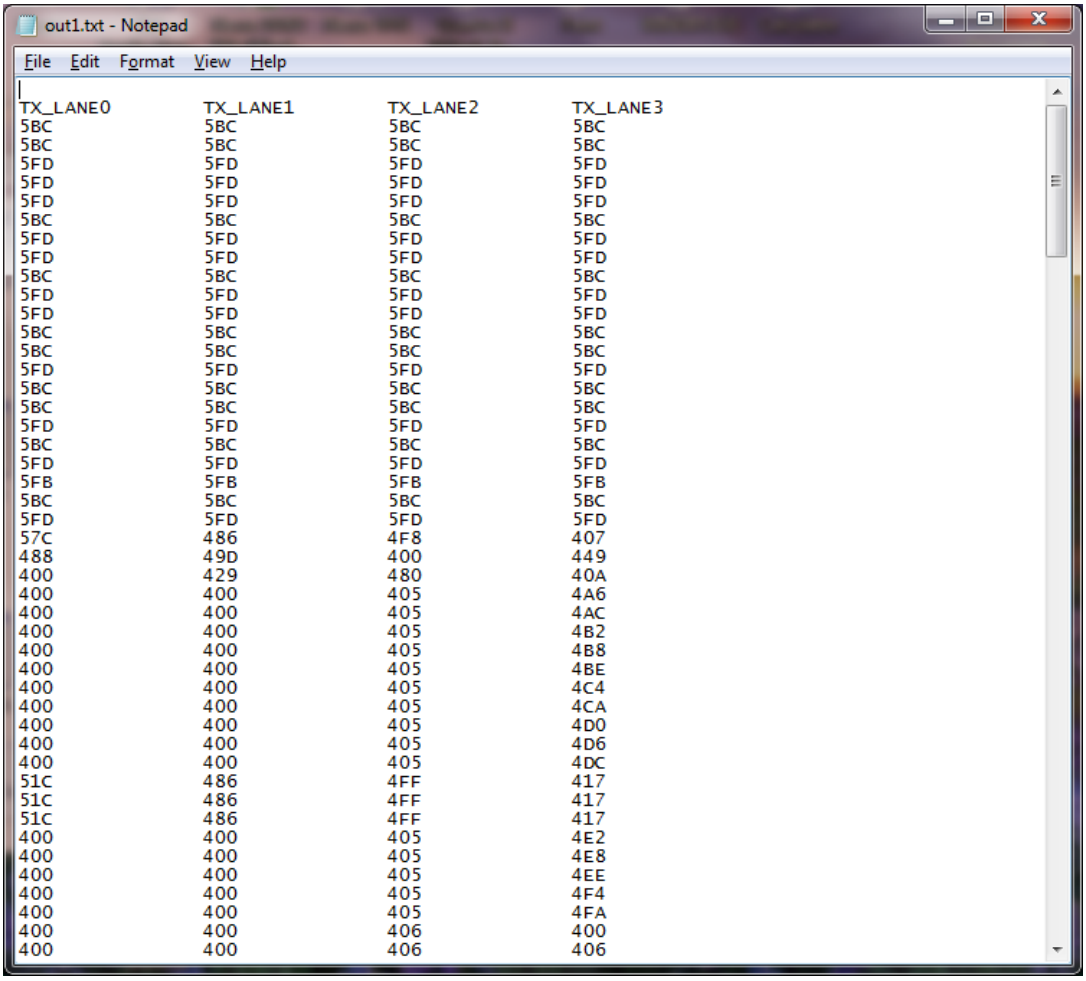

Figure 22 - Exported TLA Data

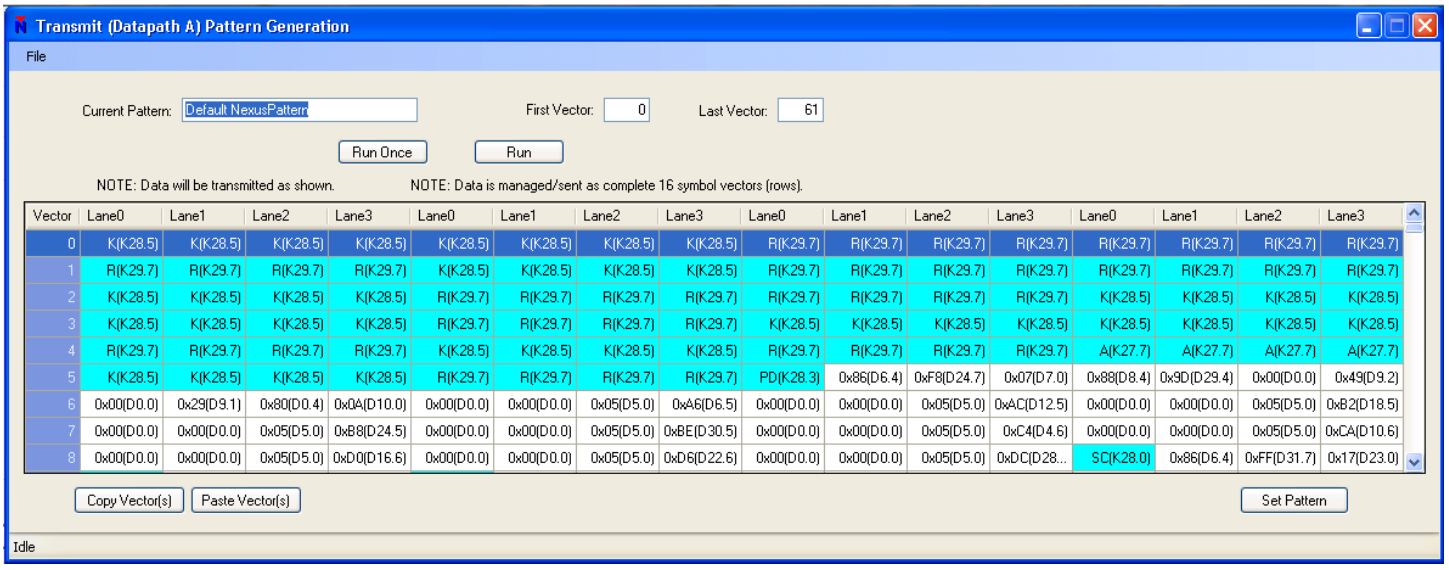

Figure 23 - Imported Data