

Memory Analyzers

MA4100 Series Memory Analyzer Datasheet



New Features!

- Supports JEDEC Engineering Procedures JEP175 DDR4 Protocol Checks published July 2017
- Updated real-time margin testing to the latest JEDEC specification JESD79-4B published June 2017
- Load-Reduced DIMM support (LRDIMM) enables up to 16 ranks per DIMM
- Second slot support enables monitoring of a dual channel with one instrument - simultaneously
- More additions to the popular real-time performance measurements
- Create your own margin tests and find elusive problems

Key Performance Specifications

- DDR4-3200
- Connects to any DDR4 target
- Continuous acquisition across clock stops and clock frequency changes
- 1G-sample acquisition depth

- Programmable probe termination
- 11ps x 10mV x 40-channel analog characterization (iCiS™)
- Real-time memory performance metrics
- Real-time memory compliance margins and validation
- Trigger in and trigger out

Key Features

- Integrated Windows 10 Controller
- Application software ready for bench, remote-to-lab or offline operation
- Application includes advanced listing, waveform, tables and charting
- Turnkey setup, including automated MRS capture and analysis
- Analyze thousands of real-time memory parameters
- Full featured, industry standard trigger system
- Automated analysis runs for everything from detailed setup information, to quick summary runs, to in-depth extended data logging or margin testing runs
- Analog eye characterization on 40-channels simultaneously at 11ps x 10mV
- Correlate with an oscilloscope for memory DQ data capture
- Patented interposer/probe designs
- Support for DIMM, SODIMM, miniDIMM, and/or x4/x8/x16 component interposers

Applications

- DDR4 and/or DDR3
 - Memory validation and debug
 - Monitoring bus traffic
 - Bus traffic measurement
 - Optimization of memory performance
 - Analog insight
- DDR4 rates to DDR4-3200
- DDR3 rates to DDR3-2667 (1.6GHz state clock capable)

Results Overview

Real-time Continuous Analysis

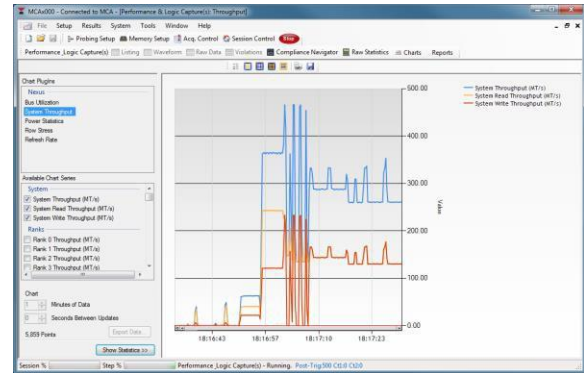
Real-time analysis provides data results during and after analysis runs which may be extremely long (days) or very short (nanoseconds). During the run, analysis is continuous and in real-time. Any event that occurs during the run is captured and analyzed.

Performance

Memory performance metrics include real-time margin metrics and margin violations. For each margin test, results indicate test coverage, observed margin values, as well as flags indicating margin violations. All data is continuously acquired in real-time with results updates continuously while the analyzer is still running.

Test	Margin	Name	Status	Min	Max	Margin	Signal Value	Description
01	OK	CS#	NA	NA	NA	512.0k	0k	Fail meet to valid command
02	OK	CS#	NA	NA	NA	512.0k	0k	Fail self refresh to command not requiring a locked DLL
03	OK	CS#_Rst	NA	NA	NA	2.0k	0k	Fail Self Refresh to ZQCL, ZQCL and MRD
04	OK	CS#_DLL	NA	NA	NA	7.0k	0k	Fail Self Refresh to command requiring a locked DLL
05	OK	CS#	NA	NA	NA	4.0k	0k	Fail power down to valid command
06	OK	CS#_RST	NA	NA	NA	8.0k	0k	Mission: clock enable during self refresh or mission self refresh time
07	OK	CS#_RST	NA	NA	NA	9.0k	0k	Check enable maximum pulse width
08	OK	CS#_RST	NA	NA	NA	70.0/200.0k	0k	Mission: power down time
09	OK	CS#_RST	NA	NA	NA	1.0k	0k	Advertise to power-down entry time
10	OK	CS#_RST	NA	NA	NA	0%	0k	Percentage single or all leads to power-down entry time
11	OK	CS#_RST	NA	NA	NA	5.0k	0k	Read with or without auto-purge to power-down entry time
12	OK	CS#_RST	NA	NA	NA	51.0k	0k	Write with a burst length of 8 to power-down entry time
13	OK	CS#_RST	NA	NA	NA	27.640%	0k	Write with auto-purge and a burst length of 8 to power-down entry time
14	OK	CS#_RST	NA	NA	NA	50.0k	0k	Write with a burst length of 4 to power-down entry time
15	OK	CS#_RST	NA	NA	NA	49.0k	0k	Write with auto-purge and a burst length of 4 to power-down entry time
16	OK	CS#_RST	NA	NA	NA	14.000%	0k	Refresh to power-down entry time
17	OK	CS#_RST	NA	NA	NA	25.0/37.5k	0k	MRD to power-down entry time
18	OK	CS#_RST	NA	NA	NA	5.0k	0k	Mission: row active time or activate to purge command period
19	OK	CS#_RST	NA	NA	NA	70.0/200.0k	0k	Mission: row active time or activate to purge command period
20	OK	CS#_RST	NA	NA	NA	83.0k	0k	Row cycle time of activate to activate/refresh command period
21	OK	CS#_RST	NA	NA	NA	0	0k	Advertise to read or write time

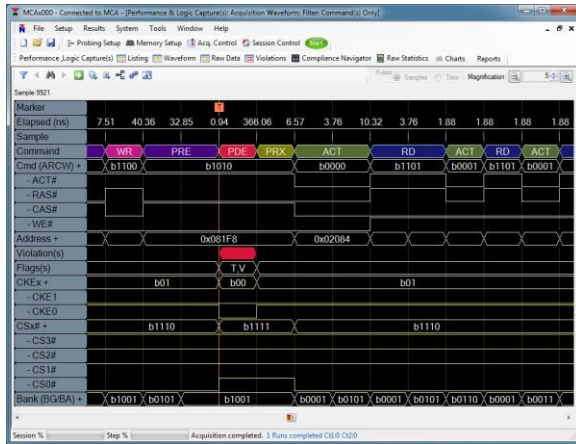
Memory performance metrics also include continuous real-time charting of bus performance characteristics such as throughput, utilization, power management, and more.



Simultaneous State Capture

State capture results include continuous traffic around one or more events of interest. The traffic - consisting of time, bus commands, bus addressing, margin violations, and trigger events - is presented in listing or waveform displays. State capture depths from one hundred samples to one billion samples is available. Advanced acquisition controls monitor and respond to the continuous traffic in real-time to best utilize the state capture memory. Advanced post-capture search and filter can quickly parse the acquisition store.

Marker	Sample	Time (ns)	Elapsed (ns)	Address	Logical Rank	Logical Rank	Command	DC	Violation(s)	Flags(s)	DDF
	913	4,051,49	3,00	0x2F0	0.0	0.2	RDB	0			b00
	915	4,052,99	1,50	0x00660	0.0	1.1	ACT	-	41: tRRC	v	b00
	918	4,055,24	2,25	0x2E8	0.0	1.2	RDB	0			b00
	924	4,059,73	4,49	0x2D0	0.0	0.2	RDB	0			b00
	930	4,064,22	4,49	0x2E8	0.0	0.2	RDB	0			b00
	936	4,068,71	4,49	0x2D0	0.0	1.2	RDB	0			b00
	942	4,073,20	4,49	0x2D0	0.0	0.2	RDB	0			b00
	948	4,077,69	4,49	0x2E0	0.0	1.2	RDB	0			b00
	954	4,082,19	4,49	0x2D8	0.0	0.2	RDB	0			b00
	960	4,086,68	4,49	0x2C8	0.0	0.2	RDB	0			b00
	966	4,091,17	4,49	0x2D0	0.0	1.2	RDB	0			b00
	979	4,100,90	9,73	0x2F8	0.0	0.3	WRB	0			b00
	983	4,103,90	2,99	0x2E0	0.0	3.1	WRB	0			b00
	987	4,106,89	3,00	0x2F0	0.0	0.3	WRB	0			b00
	993	4,109,89	2,99	0x2F0	0.0	1.3	WRB	0			b00
	995	4,112,88	3,00	0x2E8	0.0	3.1	WRB	0			b00
	999	4,115,87	2,99	0x2E8	0.0	1.3	WRB	0			b00
	1,003	4,118,87	3,00	0x2D0	0.0	2.0	WRB	0			b00
	1,006	4,121,11	2,25	-	0.0	0.2	PRE	-			b00
	1,008	4,122,61	1,50	0x2F8	0.0	1.3	WRB	0			b00
	1,012	4,125,61	2,99	0x2D8	0.0	2.0	WRB	0			b00
	1,014	4,127,10	1,50	0x2E0	0.0	1.2	PRE	-			b00
	1,016	4,128,60	1,50	0x2E0	0.0	1.3	WRB	0			b00
	1,022	4,133,09	4,49	0x2C8	0.0	1.1	WRB	0			b00
	1,026	4,136,09	3,00	-	0.0	0.3	PRE	-			b00

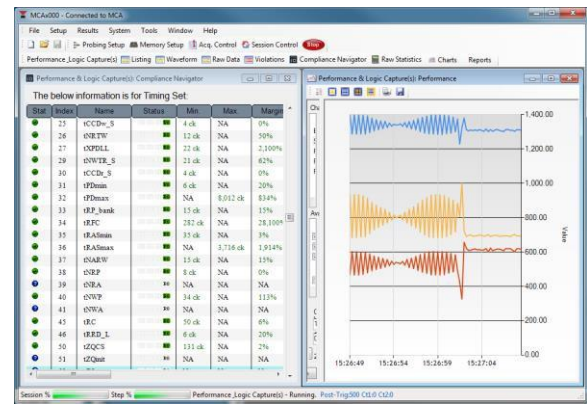
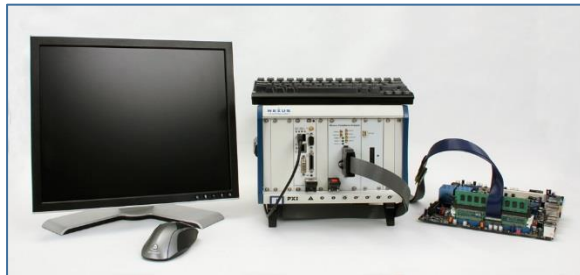


Automated Analysis

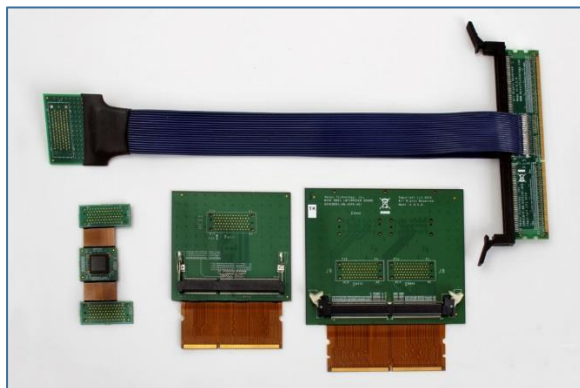
Analysis is automated and continuous from the time the user clicks the Start button until the analysis session completes. While running, the session updates the application with real-time results. In the following image you can see real-time margins for all compliance parameters as well as a chart of read/write bus throughput. In this example, the analyzer is configured to continuously monitor acquire data until the first occurrence of a compliance violation occurs. That's three simultaneous measurements, each collecting/monitoring real-time data!

Reliable Connection

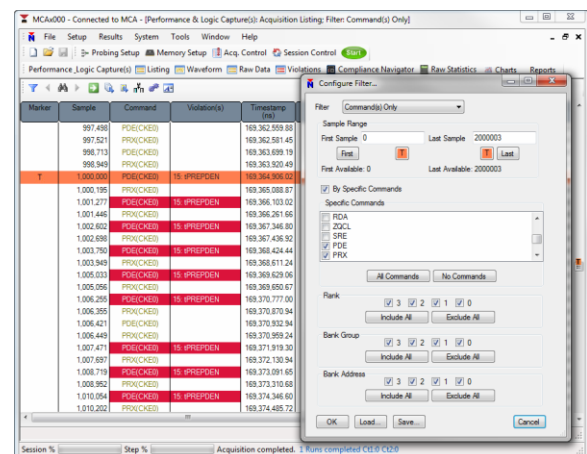
Over twenty compatible interposers/probes are available for DDR4 and DDR3 designed to preserve analog signal characteristics and maintain compatibility with Tektronix equipment for DQ data bus analysis.

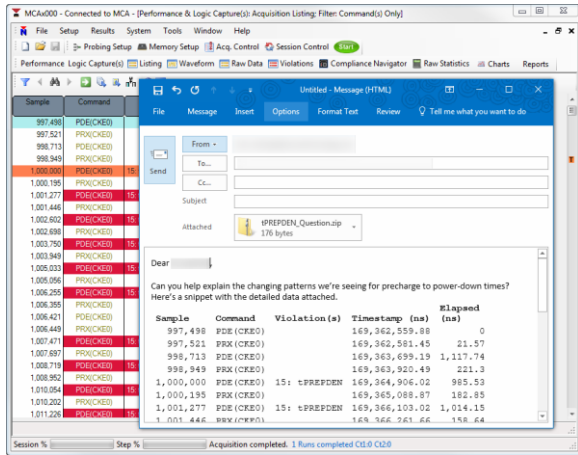


Interposers/probes available for DDR4 and DDR3 DIMMs, SODIMMs, miniDIMMs and components (x4, x8, or x16).



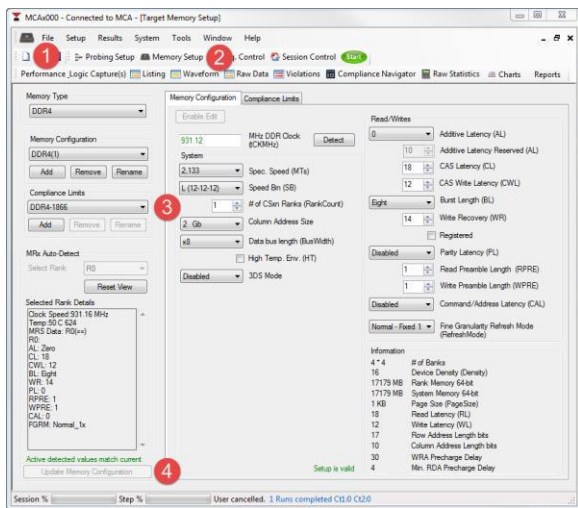
Quickly find, analyze and share intermittent problems.





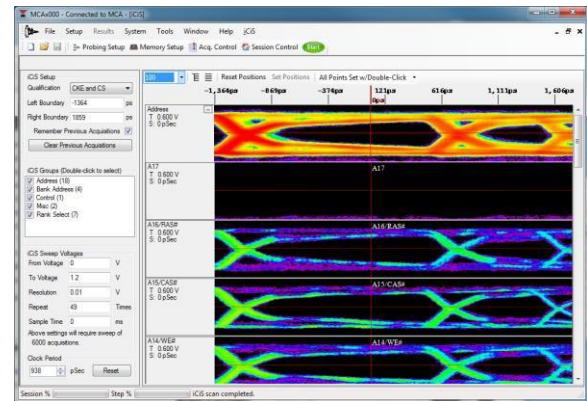
Turnkey Setup

From first starting the software there are five easy steps to start gathering data. First click the New icon (1) and select the system file for the interposer/probe you are using. Next reset your target to ensure MRS data is sent. The analyzer will automatically acquire this information! Now click the Memory Setup button (2) to display the setup window. Then select the correct speed bin, rank count, and density (3). Last, click the Update Memory Configuration button (4) to apply the MRS data to the analyzer's setup. That's it. You are ready to start analyzing data!



Higher speed operation (clock rates above 1GHz) may require additional per channel

tuning using iCiS™. For all speeds iCiS™ can also analyze whether bit errors can be expected over a configurable amount of time (from milliseconds to hours). iCiS™ is an extra step that is not always required but provides detailed and invaluable insight of signal quality and expected performance for data acquisition you can trust.



Check Online for More Information

Check online at www.nexustechnology.com for more information including video tutorials and whitepapers. Topics include:

- Oscilloscope Correlation
- TLA/Scope Correlation
- JEDEC Protocol Compliance Analysis
- Dual Instrument Architecture
- Detailed Interposer/Probe Information
- iCiS
- Triggering and State
- Violations and Margins
- And more

Available Configurations

DDR4 Configurations

NEX-MA4150-DDR4

Memory analyzer with DDR4 performance, margins and capture up to DDR4-3200 (1.6GHz) with 1G-Sample acquisition depth. Additional support for DDR3 available as an option.

NEX-MA4120-DDR4

Logic analyzer capture only up to DDR4-3200 (1.6GHz) with 512M-Sample acquisition depth. Options available for 1G-Sample, performance, and margins. Options also available to add DDR3 support.

NEX-MA4100-DDR4

Entry level memory analyzer with DDR4 performance, margins and capture up to DDR4-2667 (1.34GHz) with 512M-Sample acquisition depth. Options include 1G-Sample, and DDR4-3200 (1.6GHz) support. Options also available to add DDR3 support.

DDR3 Configurations

NEX-MA4100-DDR3

Memory analyzer with DDR3 performance,

margins and capture up to DDR3-2133 (1.34GHz capable) with 512M-Sample acquisition depth. Option for 1G-Sample. Options also available for 1.6GHz state speed. Options also available to add DDR4 support at DDR4-2667 or DDR4-3200.

Contact Information

For more information, please contact us by telephone, email or mail as listed below. Normal business hours are 9:00 - 5:00 EDT/EST.

Web	www.nexustechnology.com
Telephone	877.595.8116
International	603.329.3083
Fax	877.595.8118
Address	78 Northeastern Blvd. Unit 2 Nashua, NH 03062
Email	support@nexustechnology.com