PGY-RFFE-EX-PD RFFE Protocol Exerciser and Analyzer

RFFE Protocol Exerciser and Analyzer

The RF Front-end control interface (RFFE) Serial bus interface is emerging as a chosen for controlling RF frond end devices. There are variety of front end devices such as Power Amplifiers (PA), Low-Nose Amplifiers (LNA), filters, switches, power management modules, antenna tuners. It is widely used in mobile devices.

PGY-RFFE-EX-PD is the leading instrument that enables the design and test engineers to test the RFFE interface for its specifications by configuring PGY-RFFE-EX-PD as master/slave, generating RFFE traffic with error injection capability, amplitude variation and decoding I3C Protocol decode packets.

Features:

- Supports RFFE2.0/2.1 Specification
- Ability to configure it as Master or Slave
- Generate different RFFE at full speed and half of full frequency speed
- Error Injection such as parity errors and ACK/NACK errors
- Variable RFFE data speeds
- Simultaneously generateRFFE traffic and Protocol decode of the Bus
- Timing diagram of Protocol decoded bus
- Listing view of Protocol activity
- Error Analysis in Protocol Decode

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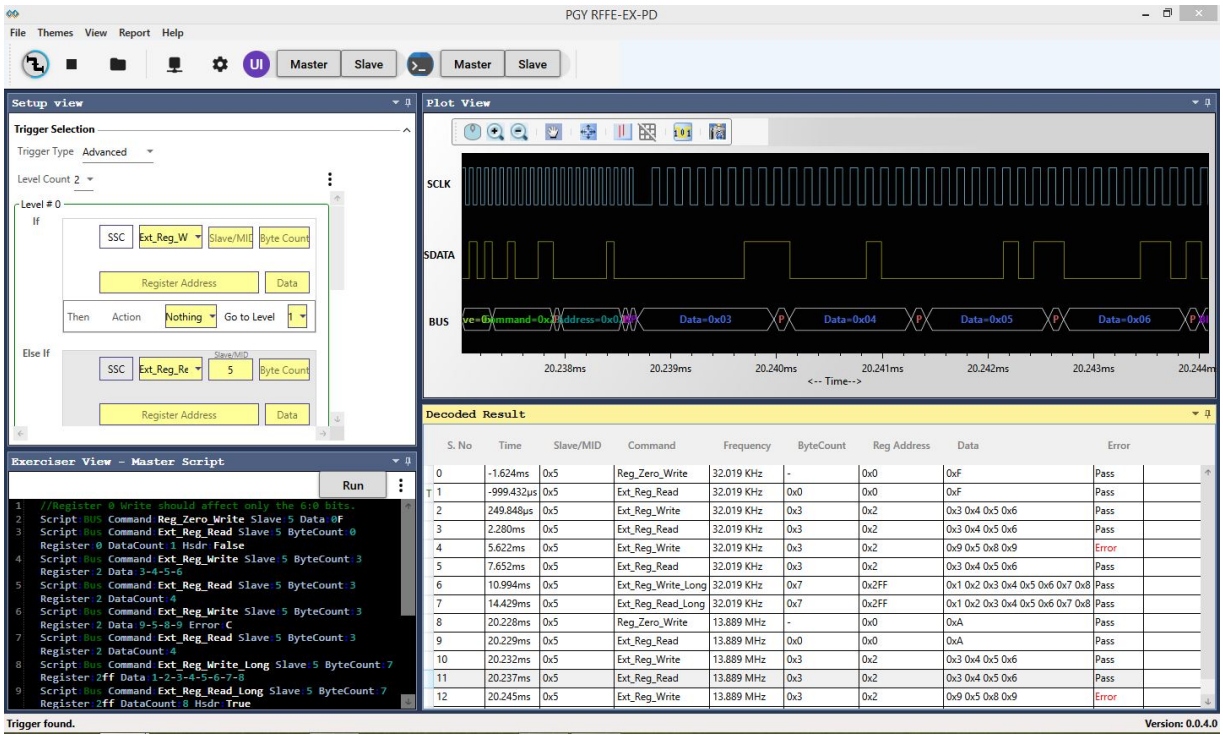
- Ability to write exerciser script to combine multiple data frame generation at different data speeds
- USB2/3 host computer interface
- Flexibility to upgrade to the unit for evolving RFFE Specification

Multi-domain View



Multidomain View provides the complete view of RFFE Protocol activity in single GUI. User can easily setup the analyzer to generate RFFE traffic using a GUI or script. User can set different trigger conditions from the setup menu to capture Protocol activity at specific event and decode the protocol transactions between Master and Slave. The decoded results can be viewed in timing diagram and Protocol listing window with autocorrelation. This comprehensive view of information makes it industry best, offering an easy to use solution to debug the I3C protocol activity.

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Exerciser:

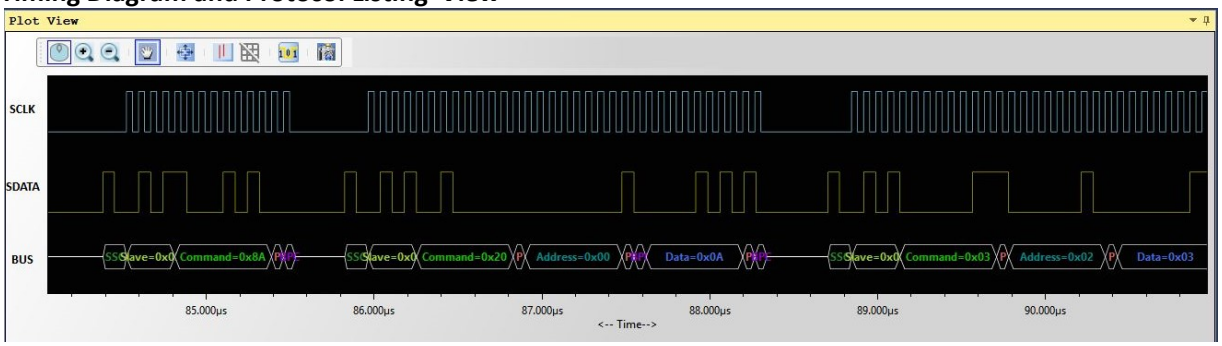
Exerciser View – Master Script

```
1  //Register 0 Write should affect only the 6:0 bits.
2  Script BUS Command Reg_Zero_Write Slave 5 Data 0F
3  Script Bus Command Ext_Reg_Read Slave 5 ByteCount 0 Register 0 DataCount 1 Hsdr False
4  Script Bus Command Ext_Reg_Write Slave 5 ByteCount 3 Register 2 Data 3-4-5-6
5  Script Bus Command Ext_Reg_Read Slave 5 ByteCount 3 Register 2 DataCount 4
6  Script Bus Command Ext_Reg_Write Slave 5 ByteCount 3 Register 2 Data 9-5-8-9 Error C
7  Script Bus Command Ext_Reg_Read Slave 5 ByteCount 3 Register 2 DataCount 4
8  Script Bus Command Ext_Reg_Write_Long Slave 5 ByteCount 7 Register 2ff Data 1-2-3-4-5-6-7-8
9  Script Bus Command Ext_Reg_Read_Long Slave 5 ByteCount 7 Register 2ff DataCount 8 Hsdr True
10 Script Sys Freq 14000 tDC 50 Volt 1.8 tIMG 0.5us
11 Script BUS Command Reg_Zero_Write Slave 5 Data 0A
12 Script Bus Command Ext_Reg_Read Slave 5 ByteCount 0 Register 0 DataCount 1 Hsdr False
13 Script Bus Command Ext_Reg_Write Slave 5 ByteCount 3 Register 2 Data 3-4-5-6
14 Script Bus Command Ext_Reg_Read Slave 5 ByteCount 3 Register 2 DataCount 4
15 Script Bus Command Ext_Reg_Write Slave 5 ByteCount 3 Register 2 Data 9-5-8-9 Error C
16 Script Bus Command Ext_Reg_Read Slave 5 ByteCount 3 Register 2 DataCount 4
```

PGY-RFFE-EX-PD supports RFFE traffic generation using GUI and Script. User can generate simple traffic generation using the GUI to test the DUT. Script based GUI provides flexibility to emulate the complete expected traffic in real world including error injections. In this sample script user can generate I3C traffic as below.

Script line #3: SET Dynamic Address using slave static
Script line #4: SETMWL with Data Parity Error
Script line #5: GETMWL with Command Parity Error
Script line #6: ENTHDR0 DDR mode with CRC Error

Timing Diagram and Protocol Listing View



Timing view provides the plot of SCLK and SDATA signals with bus diagram. Overlaying of Protocol bits on the digital timing waveform will help easy debugging of Protocol decoded data. Cursor and Zoom features will make it convenient to analyze Protocol in timing diagram for any timing errors.

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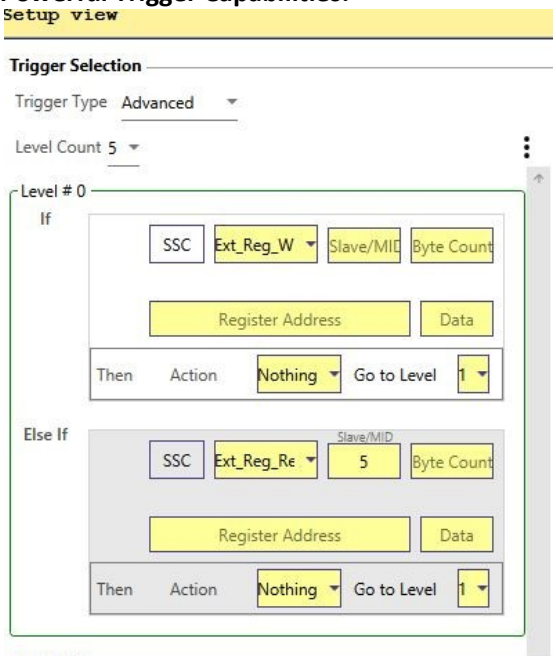
Decoded Result

S. No	Time	Slave/MID	Command	Frequency	ByteCount	Reg Address	Data	Error
0	-3.708µs	0x5	Reg_Zero_Write	13.889 MHz	-	0x0	0xF	Pass
1	-2.268µs	0x5	Ext_Reg_Read	13.889 MHz	0x0	0x0	0xF	Pass
2	612.000ns	0x5	Ext_Reg_Write	13.889 MHz	0x3	0x2	0x3 0x4 0x5 0x6	Pass
3	5.292µs	0x5	Ext_Reg_Read	13.889 MHz	0x3	0x2	0x3 0x4 0x5 0x6	Pass
4	12.996µs	0x5	Ext_Reg_Write	13.889 MHz	0x3	0x2	0x9 0x5 0x8 0x9	Error
5	17.676µs	0x5	Ext_Reg_Read	13.889 MHz	0x3	0x2	0x3 0x4 0x5 0x6	Pass
6	25.380µs	0x5	Ext_Reg_Write_Long	13.889 MHz	0x7	0x2FF	0x1 0x2 0x3 0x4 0x5 0x6 0x7 0x8	Pass
7	33.300µs	0x5	Ext_Reg_Read_Long	13.889 MHz	0x7	0x2FF	0x1 0x2 0x3 0x4 0x5 0x6 0x7 0x8	Pass
8	67.256µs	0x5	Reg_Zero_Write	13.889 MHz	-	0x0	0xA	Pass
9	68.696µs	0x5	Ext_Reg_Read	13.889 MHz	0x0	0x0	0xA	Pass
10	71.576µs	0x5	Ext_Reg_Write	13.889 MHz	0x3	0x2	0x3 0x4 0x5 0x6	Pass
11	76.256µs	0x5	Ext_Reg_Read	13.889 MHz	0x3	0x2	0x3 0x4 0x5 0x6	Pass
12	84.032µs	0x5	Ext_Reg_Write	13.889 MHz	0x3	0x2	0x9 0x5 0x8 0x9	Error
13	88.712µs	0x5	Ext_Reg_Read	13.889 MHz	0x3	0x2	0x3 0x4 0x5 0x6	Pass

Protocol window provides the decoded packet information in each state and all packet details. Selected frame in Protocol listing window will be auto-correlated in timing view to view the timing information of the packet.

Powerful Trigger Capabilities:



PGY-RFFE-EX-PD supports Auto, simple and advanced trigger capabilities. Analyzer can trigger on any of the Protocol packets such as Ext. Reg. Write, Ext. Reg, read and so forth message. Advanced Trigger provides the flexibility to monitor Multiple trigger conditions and can set multiple state trigger machine.

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PGY-RFFE-EX-PD Specification	
Excerciser:	
Configurable	1 Master+ Four Slaves OR
RFFE Traffic generation	Custome RFFE Traffic Generation
	Simulate real world network traffic
SCLK Frequency	400KHz to 13.5MHz
Voltage drive level	1 V to 3.3V at steps of 100mV
SCL Duty Cycle variation	User Define
SCL and SDA Delay	User Define
Delay between two messages	User Define
Error Injection	Parity Error injection
Protocol Analysis	
Supoorts	RFFE2.0/2.1 Protocol Decode
Protocol views	Timing Diagram view
	Protocol Listing View
	Bus Diagram to display Protocol packets with timing diagram plot
Protocol Trigger	Auto (Trigger on Any Packet)
	Simple (Triiger on any user defined I3C or I2C packet)
	Advanced (Multistate and Multilevel Trigger with Timer Capability)
Capture Duration	Continious streaming Protocl data to Host HDD/SSD
Protocol Error Report	PARITY
Host Coonectivity	USB3.0/2.0 interface

Ordering Information

PGY-RFFE-EX-PD RFFE Protocol Exerciser and Analyzer

Deliverables:

PGY-RFFE-EX-PD Unit
USB3.0 cable
PGY-RFFE-EX-PD Software in CD
12V DC adopter
Flying lead probe cable with female connector to connect to DUT

Contact:

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Prodigy Technovations Pvt Ltd (www.prodigytechno.com) is a leading global technology provider of Protocol Decode, and Physical layer testing solutions on test and measurement equipment. The company's ongoing efforts include successful implementation of innovative and comprehensive protocol decode and physical Layer testing solutions that span the serial data, telecommunications, automotive, and defense electronics sectors worldwide.