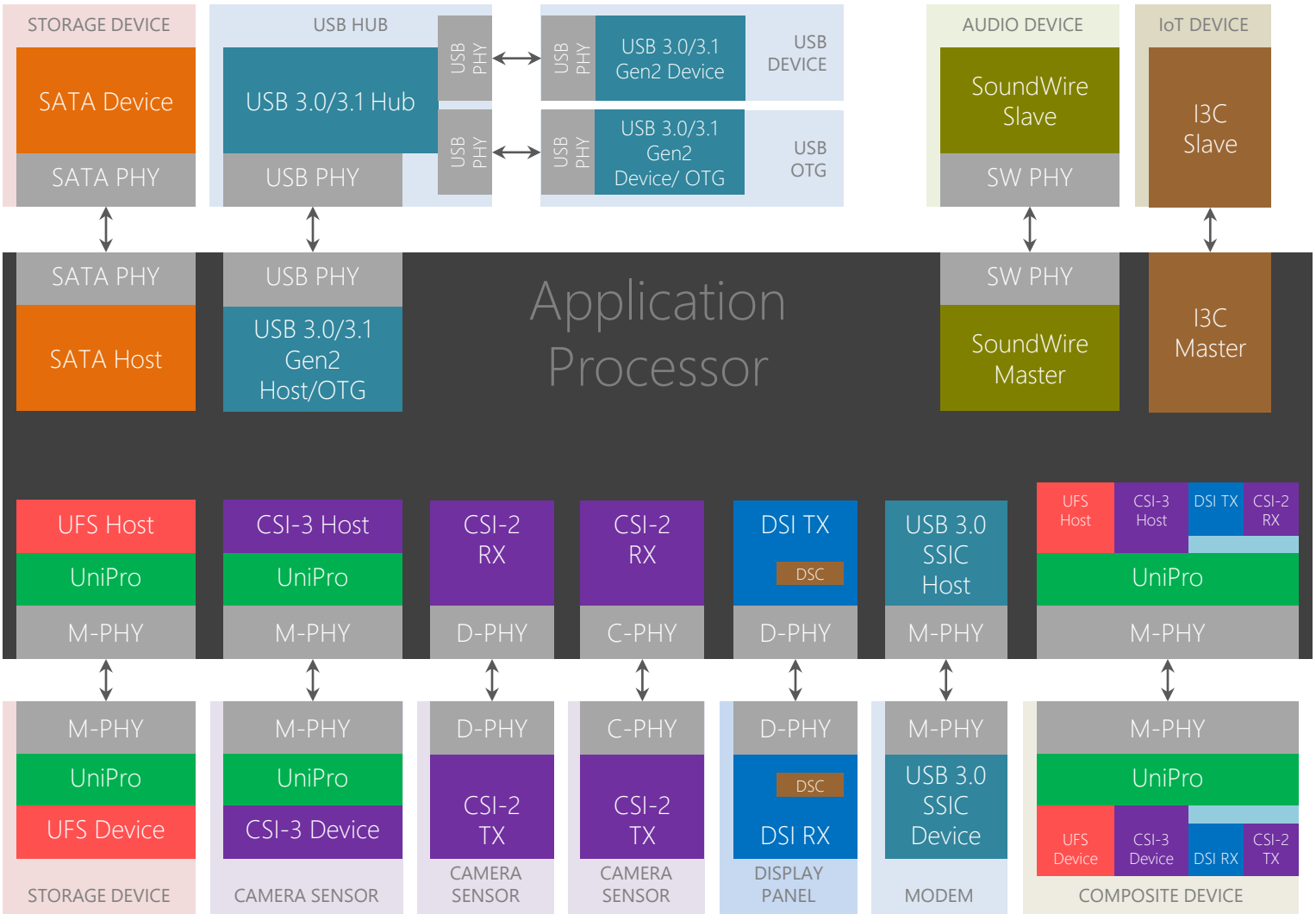
L&TTS IP Portfolio

(former GDA Technologies)

L&T Technology Services offers ASIC/FPGA IPs and Total System Solutions for those IPs that includes Validation and Design Platforms, Software and Drivers, etc. In addition, LTTS provide larger Silicon, System and End-Product design services. LTTS specialize in large high speed designs that require technological excellence and is an early adopter of multiple products.

TOTAL SOLUTION – CONTROLLER, PHY, SOFTWARE, PLATFORM

- CSI-2 TX & RX for CPHY-DPHY Combo
- DSI & DSI-2 TX & RX for DPHY
- CSI-3 Host and Device
- UFS Host and Device
- I3C Master and Slave
- SoundWire Master and Slave
- USB 3.0/3.1 Gen2 Host, Device, Hub
- USB 3.0 Dual Mode, OTG, SSIC
- SATA 6G Host



L&TTS MIPI CSI-2 TX & RX Controller

CAMERA IMAGING

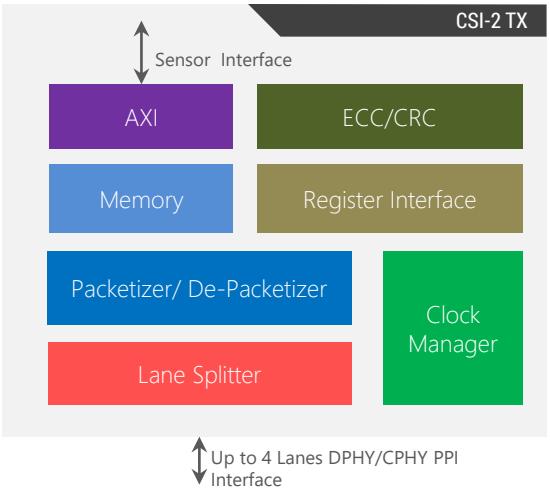
PRODUCT BRIEF

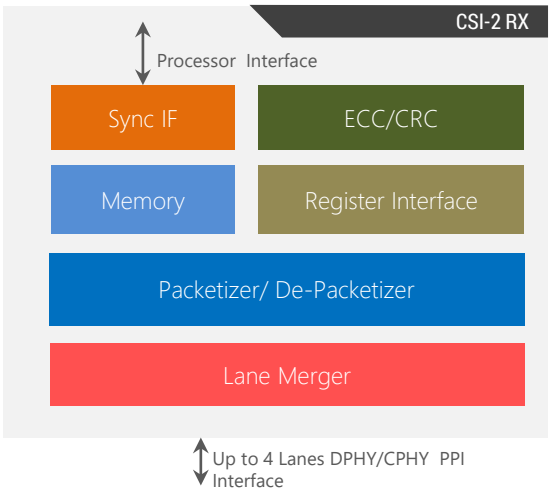
The MIPI Camera Serial Interface (CSI-2) is an interface between a Camera or image processing engine. This interface is defined by MIPI Alliance, which defines a series of modules in a MIPI compliant product.

L&T MIPI CSI-2 Receiver is used in mobile and high–speed serial applications as a controller for receiving video, command or user data transmitted using MIPI CSI-2 Transmitter over MIPI lines. It is sent to the next higher level for subsequent processing. The L&T MIPI CSI-2 Receiver along with L&T MIPI CSI-2 Transmitter and MIPI DPHY/CPHY provides a complete solution for MIPI CSI-2 communication.

FEATURES

- Compliant with MIPI CSI Standard v2.x and MIPI D-PHY Standard v1.x, MIPI D-PHY Standard V2.x and MIPI C-PHY V1.x
- Up to 3 Gsps per trio using C-PHY. 17Gbps in 3 Trios.
- Up to 2.5 Gbps per data lane of D-PHY (V2.0). 10Gbps in 4 Lanes
- Programmable 1, 2, 3 (C-PHY) or 4 (D-PHY) Data Lane Configuration.
- Configurable up to 4 Virtual Channels
- Operate in continuous and non-continuous clock modes.
- Color Modes: 16, 18, 24 and 36 bpp
- Color Formats: YUV420 8, 10bits and without CSPS and Legacy, YUV422 8, 10bits, RGB-888, 565, 666, 555 and 444. RAW6, 7, 8, 10, 12 and 14.
- Register configuration through CCI interface
- Host Interface can be Pixel or AXI interface.





CONFIGURABLE OPTIONS

- Data Lane Count
- Color modes
- Pixel interface width
- Application Interface – Pixel, AXI
- Command FIFO depth
- Data Lane Count

DESIGN ATTRIBUTES

- Highly modular and configurable design
- Layered architecture
- Active low async reset
- Clearly de-marked clock domains
- Extensive clock gating support

PRODUCT PACKAGE

- Configurable RTL Code
- HDL based test bench and behavioral models
- Test cases
- Protocol checkers, bus watchers and performance monitors
- Configurable synthesis shell
- Documentation
  - Design Guide
  - Verification Guide
  - Synthesis Guide

L&TTS MIPI DSI TX & RX Controller

PRODUCT BRIEF

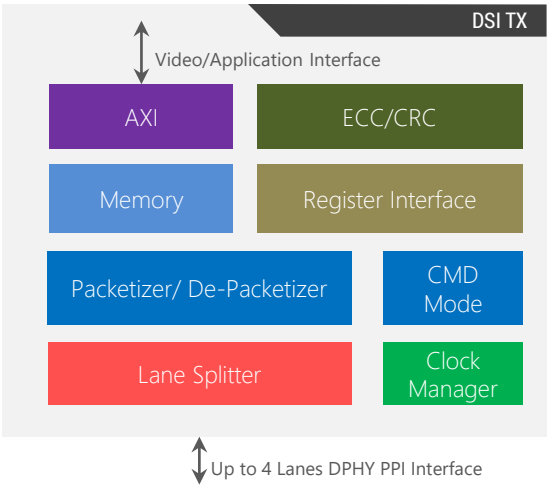
DISPLAY IMAGING

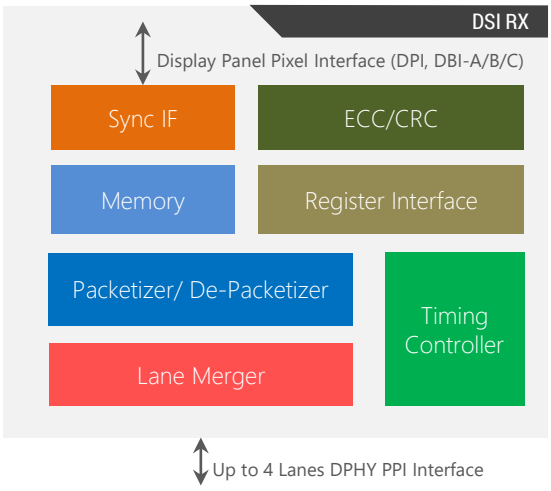
The MIPI Display Serial Interface (DSI) is an interface between a Display or other data interface and a host processor baseband application engine. This interface is defined by MIPI Alliance, which defines a series of modules in a MIPI compliant product.

L&T MIPI DSI Receiver is used in mobile and high–speed serial applications as a controller for receiving video, command or user data transmitted using MIPI DSI Transmitter over MIPI lines. It is sent to the next higher level for subsequent processing. The L&T MIPI DSI Receiver along with L&T MIPI DSI Transmitter and MIPI DPHY provides a complete solution for MIPI DSI communication.

FEATURES

- Compliant with MIPI DSI-2 Standard v0.8.x, MIPI D-PHY Standard v1.x, MIPI D-PHY Standard V2.x and MIPI C-PHY V1.x
- Up to 3 Gsps per trio using C-PHY. 17Gbps in 3 Trios.
- Up to 2.5 Gbps per data lane of D-PHY (V2.0). 10Gbps in 4 Lanes
- Programmable 1, 2, 3 (C-PHY) or 4 (D-PHY) Data Lane Configuration.
- Forward and Reverse Communication
- Configurable Virtual Channel up to 4
- Operate in continuous and non-continuous clock modes.
- Command and Video Mode are supported.
- Burst and Non-Burst modes are supported.
- Pulse and Event modes supported
- Color Modes: 16, 18, 24 and 36 bpp
- Display Stream Compression (DSC) Supported





CONFIGURABLE OPTIONS

- Data Lane Count
- Color modes
- Pixel interface width
- Application Interface – Pixel, AXI
- Command FIFO depth
- Data Lane Count

DESIGN ATTRIBUTES

- Highly modular and configurable design
- Layered architecture
- Active low async reset
- Clearly de-marked clock domains
- Extensive clock gating support

PRODUCT PACKAGE

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  - Synthesis Guide

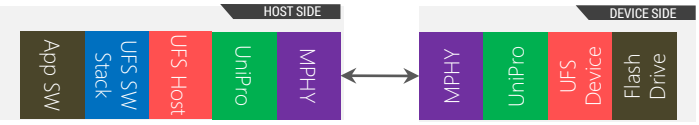
L&TTS UFS Host & Device Controllers

PRODUCT BRIEF

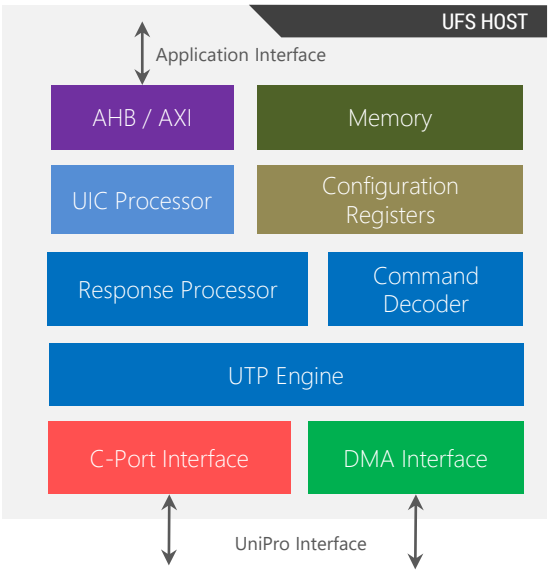
STORAGE SOLUTIONS

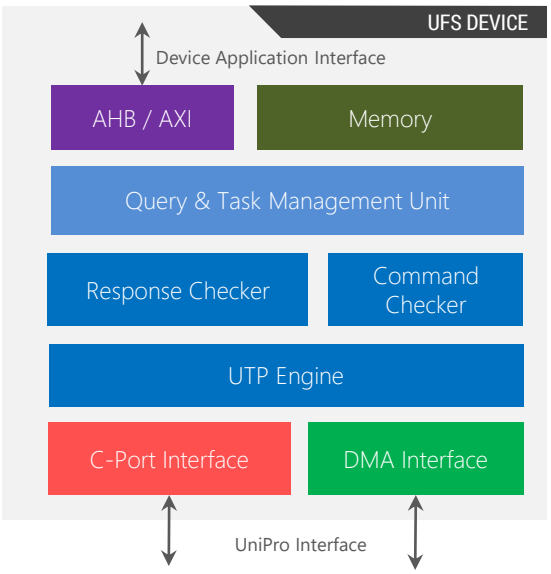
UFS is a high performance, serial interface used in mobile systems as a mechanism to communicate between host processor and mass storage devices like Flash and other non-volatile memories. This communication is achieved using a UFS Host and UFS Device, using MIPI UniPro and MPHY as Link and PHY layers respectively. UFS Host controller interface is responsible for managing the interface between host software and UFS device to do a data transfer. It also does the interface management, power management and control.

L&TTS UFS Host works perfectly with any UFS Device and vice versa along with L&TTS MIPI UniPro and partner MPHY. With this, L&TTS provides the complete solution including software and Validation platform.



- Compliant with UFS Specification v2.x
- Supports up to 2-lanes (restricted by Standard) running at HS-G3 (5.8Gbps)
- AXI Support
- All UPIU Processing
    - Datain, Dataout, Command, Response, RTT, Query, Task Management and Reject
- Complete control of UIC Layer by UFS Host
- Error Reporting and Handling Supported
- Priority arbitration between command, query and task management UPIUs and Indexed based processing within Command and Query UPIUs.
- Supports 32 UTP Transfer request descriptors and 8 UTP Task Management Descriptors for UFS host
- Supports Boot LUN, RPMB Well-known LUNs.
- Device: Up to 8 LUNs configurable. Up to 8 command queue in each LUN. Up to 8 tasks handling for task management.
- Priority LUN handling.
- Security Features





CONFIGURABLE OPTIONS

- C-Port
- Application Interface – APB, AXI

DESIGN ATTRIBUTES

- Highly modular and configurable design
- Layered architecture
- Supports both sync and async reset
- Clearly de-marked clock domains
- Extensive clock gating support
- Multiple Power Well Support
- Software control for key features

PRODUCT PACKAGE

- Configurable RTL Code
- HDL based test bench and behavioral models
- Test cases
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    - Synthesis Guide

L&TTS UniPro Controller

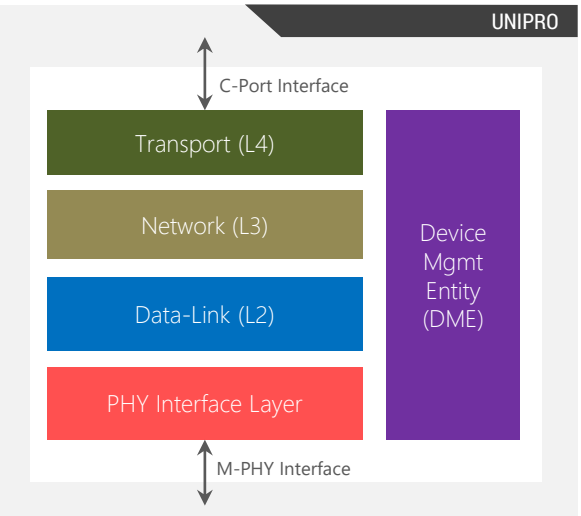
PRODUCT BRIEF

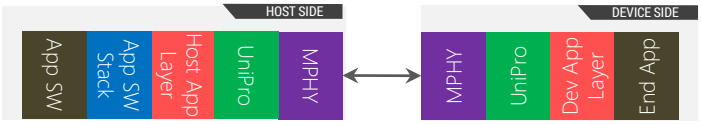
INTERFACE SOLUTIONS

UniPro (Unified Protocol) is a layered protocol defined by MIPI Alliance for interconnecting devices and components within a mobile device. UniPro enables the components of a device to utilize MIPI PHY layer, like MPHY to communicate and exchange data to devices on the other side of MIPI lanes. UniPro supports a wide range of device applications like application processor, camera controller, display controllers, storage controllers like UFS, memory (RAM) controllers etc.

LTTS MIPI UniPro is designed to be PHY agnostic and can support a wide range of multiple applications simultaneously in the application layer. LTTS MIPI UniPro along with LTTS's Application solutions like CSI-3 or UFS and Our partner's MPHY forms a complete solution to your needs.

- Compliant with MIPI UniPro Standard V1.6x and MPHY standard 3.x
- Programmable 1, 2, or 4 data lanes
- Supports M-PHY HS data rates HS-Gear-1,Gear-2, Gear-3, both A/B modes and PWM data rates PWM-G1 to PWM-G7
- Supports End to End flow control.
- Supports all traffic classes.
- Supports preemption of high priority frames.
- Supports maximum of 32 C-Ports.
- Employs Round Robin arbitration across C-Ports.
- Supports group acknowledgement of maximum 16 frames per traffic class.
- Supports retransmission of frames.
- Configurable buffer spaces.
- Supports CSD, CSV.
- Supports UniPro Test Feature.
- TMPI Support.
- Efficient Power Management





CONFIGURABLE OPTIONS

- C-Port
- Number of Lanes

DESIGN ATTRIBUTES

- Highly modular and configurable design
- Layered architecture
- Supports both sync and async reset
- Clearly de-marked clock domains
- Extensive clock gating support
- Multiple Power Well Support
- Software control for key features

PRODUCT PACKAGE

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L&TTS SoundWire Master & Slave Controllers

AUDIO SOLUTIONS

PRODUCT BRIEF

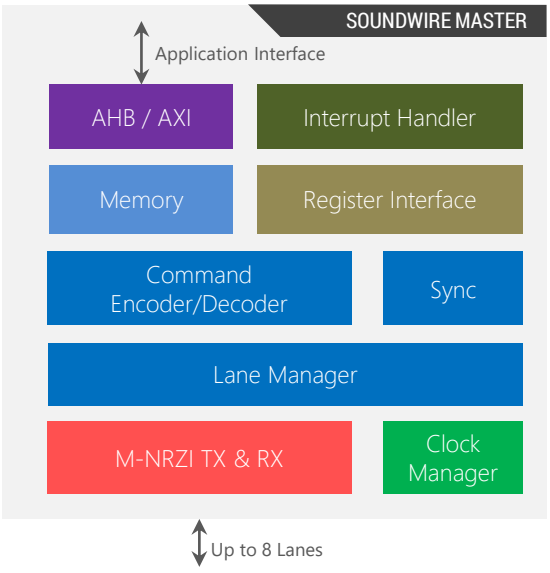
The MIPI SoundWire is an interface specification that enables bi-directional digital Audio communication between a Master and one or more slave devices and among slave devices. It is optimized for mobile and Mobile inspired systems. It can co-exist with MIPI-Compliant and non-MIPI-Compliant devices.

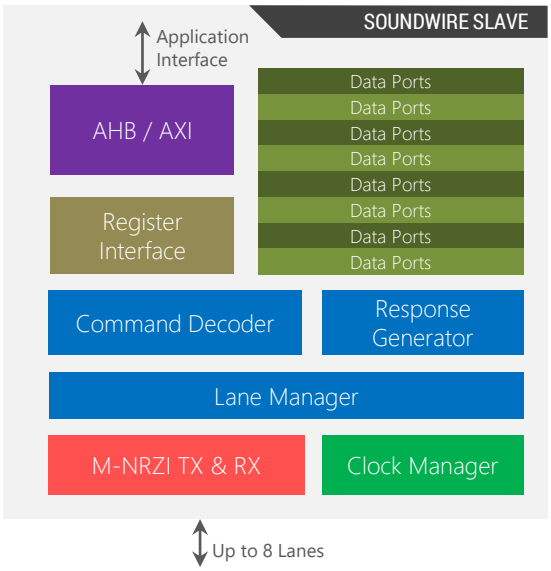
MIPI SoundWire is low-complex, low-power, low-latency interface that supports multi-channel data. Being low gate count enables it to be adopted it into smaller components like microphones and amplifiers.

L&T's SoundWire Master is used in any master controllers like Amplifiers or processors to transfer or receive audio data from one of the SoundWire slaves, like the one connected to a microphone or a speaker. Likewise L&T's SoundWire Slave is a full SoundWire standard compliant slave that can do a slave to slave communication according to the device component connected to it.

FEATURES

- Compliant with MIPI SoundWire Standard 1.x
- L&TTS SoundWire Host can support up to 11 Slaves.
- Up to 8 Data Lanes supported
- Slave-to-Slave transport supported
- Modified-NRZI Data Encoding.
- Special internal register space for each devices
- Optional Monitor Interface
- Optional APB/AXI interface supported.
- Configurable data width: 8/16/32-bit





CONFIGURABLE OPTIONS

- PDI Count, Width, Type
- Application Interface – APB, AXI
- Command FIFO depth
- Data Lane Count
- Data Port Memories

DESIGN ATTRIBUTES

- Highly modular and configurable design
- Layered architecture
- Supports both sync and async reset
- Clearly de-marked clock domains
- Extensive clock gating support
- Multiple Power Well Support
- Software control for key features

PRODUCT PACKAGE

- Configurable RTL Code
- HDL based test bench and behavioral models
- Test cases
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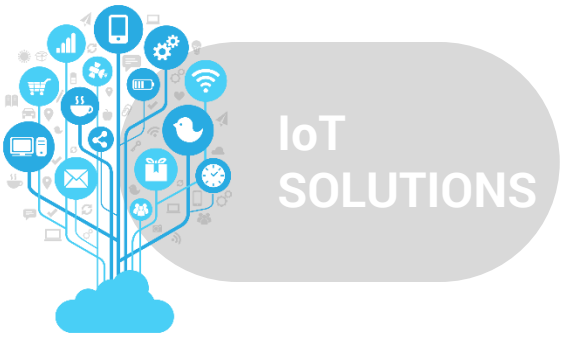
  - Synthesis Guide

L&TTS I3C Master & Slave Controllers

PRODUCT BRIEF



I3C interface is a fast, low cost, low power, two wire digital interface for sensors in mobile wireless products. L&T's I3C supports several communication formats all sharing a two wire interface - SDA and SCL. SDA is a bidirectional data pin while SCL can be either a clock pin or a data pin while in HDR mode. The type of communication supported by L&T's I3C

- I2C-like communication with SCL clock speed up to 12.5 MHz
- MIPI-defined transmissions that allow the master to communicate to one or all slaves on the bus.
- HDR mode using ternary number symbols to achieve two data transmissions per equivalent clock cycle.
- A subset of I2C communication to legacy I2C slaves, if present on the bus.
- Slave initiated request to master, e.g. In-band interrupt, address request.

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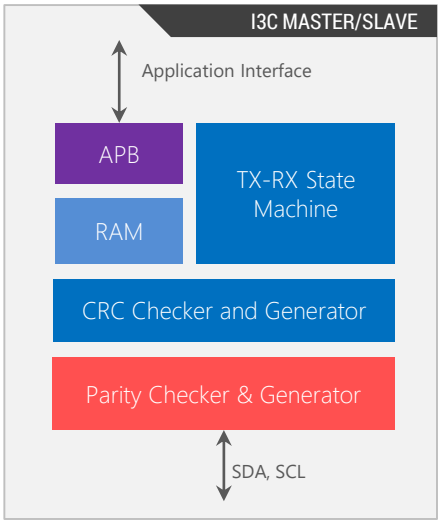

FEATURES

- Compliant with the MIPI Alliance Draft Specification for I3C Version 0.5 Revision 1
- I3C Master Features
  - Supports all modes of Master – SDR, HDR and HDR-DDR,I2C Modes
  - Can be configured to work as secondary master also.
  - Dynamic addressing assignment capability
  - Support for slave generated inband interrupts.
  - Memory for retaining bus device addresses.
- I3C Slave Features
  - Supports I3C slave configuration – HDR-DDR Slave, SDR Only Slave.
  - Common Slave IP can be instantiated many times to have multiple slaves on the I3C bus.
  - Dynamic address complaint.
  - Supports/Tolerate I3C global command codes.
- Master Interface for system access : APB. Optionally AXI.
- Slave Interface for Register access : APB
- Configurable FIFOs

CONFIGURABLE OPTIONS

- I3C Master Can be configured to work as secondary master.
- I3C Slave configuration – HDR-DDR Slave, SDR only Slave.
- System Access: APB or AXI
- Configurable FIFO's

DESIGN ATTRIBUTES

- Highly modular and configurable design
- Supports both sync and async reset
- Software control for key features

PRODUCT PACKAGE

- Configurable RTL Code
- HDL based test bench and behavioral models
- Test cases
- Protocol checkers, bus watchers and performance monitors
- Configurable synthesis shell
- Documentation
  - Design Guide
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  - Synthesis Guide

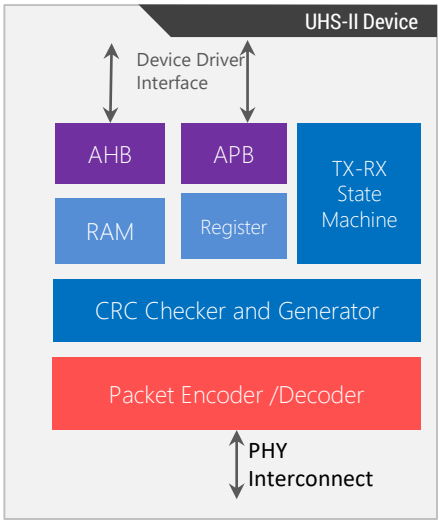
L&TTS UHS-II Device

PRODUCT BRIEF

STORAGE SOLUTIONS

UHS-II is Ultra High speed type II controller for high speed transfers used in SD application for High definition contents. Key factors includes reusability of legacy resources, low voltage ,low power consumption and low EMI used in mobile devices. The type of connection topology supported by L&T's UHS

- Full Duplex Mode(FD mode) - Lane consists of one Transmitter port, Receiver Port and transmission clock. Data rate up to 156MB/s
- Half Duplex with 2lanes mode(2L-HD Mode)- Changes the lane directions to 2lane mode during data transfer to achieve data rate up to 312MB/s.
- Full Duplex with 2 Downstream and 1 upstream lane mode (2D1U-FD Mode)
- Full Duplex with 1 Downstream and 2 upstream lane mode (1D2U-FD Mode)
- Full Duplex with 2 Downstream and 2 upstream lane mode (2D2U-FD Mode)



FEATURES

- Compliance with Part 1 UHS-II Addendum Version 1.02
- Compliance with Part A2 SD Host controller specification version 4.10 & Part1 Physical layer specification version 4.20
- Programmable 1 or 2 Data lane Configuration
- Supports all type of packets
- Compatibility with Legacy SD interface
- APB for Register configuration
- AHB for Read/Write Data Transfer
- Supports fast mode and low power mode
- Supports flow control operations.
- Supports command Queuing, Relaxed Ordering and inter-device communication
- Supports data transaction for SD-TRAN and CM-TRAN
- Configurable FIFOs

CONFIGURABLE OPTIONS

- UHS Device configuration – HD, FD, 2D1U-FD, 1D2U-FD, 2D2U-FD Mode
- System Access: APB or AHB or AXI
- Configurable FIFO's

DESIGN ATTRIBUTES

- Highly modular and configurable design
- Supports both sync and Async reset
- Software control for key features

PRODUCT PACKAGE

- Configurable RTL Code
- UVM based test bench and behavioral models
- Test cases
- Protocol checkers, bus watchers and performance monitors
- Configurable synthesis shell
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  - Synthesis Guide

L&TTS USB 3.x Hub Controller

PRODUCT BRIEF

USB 3.0/3.1 SOLUTIONS

LTTS are pioneers in USB controller Solutions. LTTS provides highly configurable and scalable USB 3.1 Host/Device/Dual-Mode controller IP Core for wide range of applications.

With a strong focus and expertise in delivering engineering services, LTTS works closely with clients in understanding their requirements, providing optimized configuration of the IP Core to meet specific requirements and in addition customizing the IP core for clients product differentiation. Extended engineering service engagements enable clients to utilize LTTS core development team to be deployed for fail safe integration of the IP in the clients SoC/end-product. All licensees are also provided with validation platforms along with necessary firmware support which can be used to functionally validate the product prior to tape-out mitigating risks.

All IP's are provided as a complete solution consisting of a comprehensive verification suite, Clock Domain Crossing, Synthesis, and Logical equivalence constraints and waivers as applicable which are reusable at SoC level, along with pre-verified and interoperate proven with partner PHY solutions

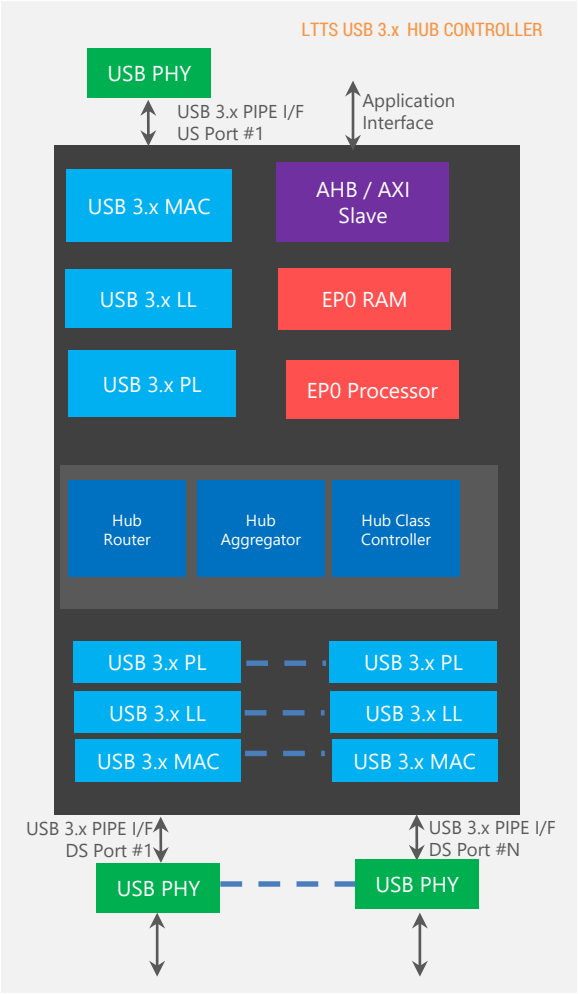
LTTS USB 3.x Hub controller are designed for compliance with USB3.1 specification, Revision 1.0 and all associated ECN's.

LTTS USB 3.x Hub Controller can be configured to support only SS mode of operation or optionally support SS/SSP mode of operation. The USB 3.x Hub Controller implements an EP0 processor, which autonomously responds to USB transaction initiated from the host and directed to it.

LTTS USB 3.x Hub Controller supports configurable number of downstream ports. LTTS USB 3.x Hub Controller implements shared configurable and efficient buffering for packets directed from/to each downstream port of the Hub. LTTS USB 3.x Hub Controller provides a simple slave AHB/AXI interface to access its internal registers.

LTTS USB 3.x Hub Controller can be easily integrated with third party USB 2.0 Hub to implement a full fledged USB 3.1 Hub.

LTTS USB 3.x Hub Controller supports full USB 3.0 power management (U1, U2, U3/suspend, remote wakeup) and additionally, supports ganged or per port power switching/overcurrent detection of the downstream ports.



PRODUCT PACKAGE

- Configurable RTL Code
- HDL based test bench and behavioral models
- Test cases
- Protocol checkers, bus watchers and performance monitors
- Configurable synthesis shell
- Documentation
  - Design Guide
  - Verification Guide
  - Synthesis Guide
- FPGA Platform for Pre-Tape-out Validation

FEATURES

- LTTS USB 3.x Hub Controller can be configured to support software and hardware configurable number of downstream ports – 1 to 16.
- Allows dynamic association between physical ports and logical ports
- LTTS USB 3.x Hub Controller can be configured to support any combinations of USB 3.x interface speeds – SSP (10 Gbps), SS(5 Gbps), SSP and SS.
- LTTS USB 3.x Hub Controller has full support for all low power features of the USB Specification supporting Suspend and Remote Wakeup, USB 3.x Low Power States – U1/U2/U3.
- LTTS USB Controllers have been Silicon Proven in wide range of products such as Graphics Controller, Flash Storage Controllers, SATA Bridges with support for Bulk Streaming, Embedded Hosts, Docking Stations, Mobile Application Processors, Smart TV, Hubs.

Compliance
- LTTS USB 3.1 Host Controller IP core is compliant with USB 3.1 specification, Revision 1.0 and all associated ECN's.

Configurability
- Support for managing configurable number of Downstream Ports
- Hardware configurable support for USB speeds – SSP and/or SS operation.
- Software configurable mapping between physical and logical ports of the Hub.
- Support for either Ganged or Per Port Overcurrent Support
- Support for either Ganged or Per Port Power Switching.

Feature Rich
- Internal data path width: 32
- External data path width: 32 / 64 bits
- USB PHY Interface
  - SS : 8/16/32-bit PIPE Interface
  - SSP : 32-bit PIPE Interface
- Efficient buffering scheme.
- Register Path Interface: AHB

DESIGN ATTRIBUTES

- Highly modular and configurable design
- Layered architecture
- Fully synchronous design
- Supports both sync and async reset
- Clearly de-marked clock domains
- Extensive clock gating support
- Multiple Power Well Support
- Software control for key features

Application Layer Features
- AHB / AXI System Slave Interface to program the EP0 RAM, to program/read the status of the internal registers of the core.
- Software configurable association between Physical and Logical Downstream Ports.
- Software configurable association for Ganged/Per Port Overcurrent Detection.
- Software configurable association for Ganged/Per Port Power Switching.
- Configurable Buffer Sizes.
- Asynchronous clocking between Hub Controller and each of the upstream and downstream ports.

Protocol and Link Layer Features
- Supports Interrupt/Bulk/Isochronous/Control Transfers.
- CRC checking and generation
- Implements Type 1 and 2 Buffers in case of USB 3.1 SSP.
- Supports LFPS Signaling and for SSP supports SCD/LBPM Messaging
- Option to enable/disable scrambling
- Supports Master and Slave Loopback mode for PHY layer testing
- Supports Compliance mode entry as per specification.
- Optional Support for Type C Connector Interface
- Implements all downstream flowing traffic ordering and buffering rules.
- Implements all upstream flowing ordering and buffering rules.
- Supports Protocol Layer Error Handling.
- Supports PTM

Register Support
- Supports CSR, PL, PM registers for Device mode of operation.
- Simple slave interface to access these registers.
- Additional design specific debug, control and status registers.

Power Management Support
- Supports USB Suspend state and supports remote wakeup devices.
- Supports all SS/SSP Link Power Management States – U1, U2, U3
- Supports system low power and related system states such as Sleep, Hibernate, Warm/ Cold boot etc.
- Support for clock gating and multi-power-well support.

L&TTS USB 3.1 Host Controller

PRODUCT BRIEF

USB 3.0/3.1 SOLUTIONS

LTTS are pioneers in USB controller Solutions. LTTS provides highly configurable and scalable USB 3.1 Host/Device/Dual-Mode controller IP Core for wide range of applications.

With a strong focus and expertise in delivering engineering services, LTTS works closely with clients in understanding their requirements, providing optimized configuration of the IP Core to meet specific requirements and in addition customizing the IP core for clients product differentiation. Extended engineering service engagements enable clients to utilize LTTS core development team to be deployed for fail safe integration of the IP in the clients SoC/end-product. All licensees are also provided with validation platforms along with necessary firmware support which can be used to functionally validate the product prior to tape-out mitigating risks.

All IP's are provided as a complete solution consisting of a comprehensive verification suite, Clock Domain Crossing, Synthesis, and Logical equivalence constraints and waivers as applicable which are reusable at SoC level, along with pre-verified and interoperate proven with partner PHY solutions

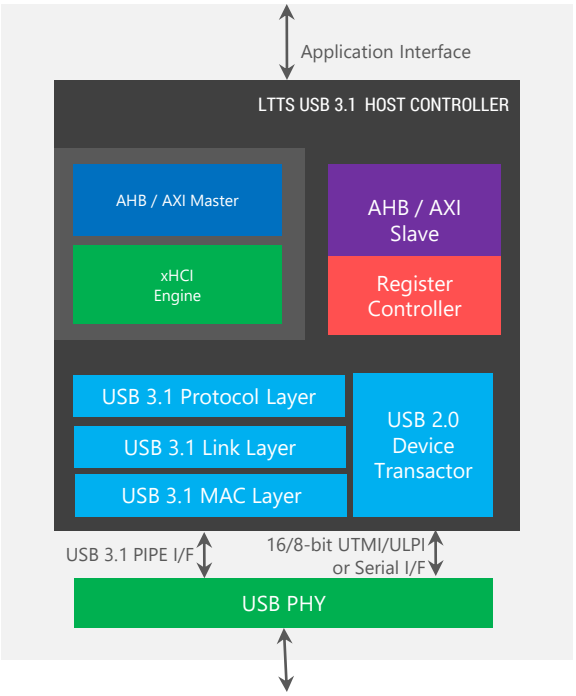
LTTS USB 3.1 controller are designed for compliance with USB3.1 specification, Revision 1.0 and all associated ECN's, USB specifications Rev 2.0 and all associated ECN's.

LTTS USB 3.1 Host controller is architected to optionally include a High Performance DMA Engine based on xHCI Specification. All buffering associated with the DMA Engine are configurable based on latency and performance requirements. The core can be configured to support full fledged xHCI implementations for use in standard PCIe-USB bus adaptors/chip sets or be configured with a subset of features for embedded applications requiring limited host functionality.

LTTS USB 3.1 Host Controller based on xHCI specification can be used in systems using any OS which provides xHCI/USB Stacks such as – Android, Linux, Windows.

LTTS USB 3.1 Host controller exposes either a AXI or AHB Master Interface for the Datapath and an AHB Slave Interface for Register Access. Optionally, a interoperate proven 3rd Party PCIe-AXI/AHB bridge can be provided for use in standard desktop / server applications.

Optionally, the controller can be provided with no xHCI Engine and no buffering and operates in a cut-through mode forwarding and receiving USB payloads and managing only the USB protocol. Customer may in this case implement its own differentiated DMA Engine. Optionally, a simple transmit and receive buffer is included in this configuration which can be accessed by software over the slave register access interface which is typically AHB. This option results in very low footprint hardware which can be used in cases where the software can completely manage the USB traffic – including the sequencing of the USB transactions.



DESIGN ATTRIBUTES

- Highly modular and configurable design
- Layered architecture
- Fully synchronous design
- Supports both sync and async reset
- Clearly de-marked clock domains
- Extensive clock gating support
- Multiple Power Well Support
- Software control for key features

PRODUCT PACKAGE

- Configurable RTL Code
- HDL based test bench and behavioral models
- Test cases
- Protocol checkers, bus watchers and performance monitors
- Configurable synthesis shell
- Documentation
    - Design Guide
    - Verification Guide
    - Synthesis Guide
- FPGA Platform for Pre-Tape-out Validation

FEATURES

- LTTS USB 3.1 Host Controller can be configured to support all types of USB transfers – Bulk, Interrupt and Isochronous.
- Allows dynamic configuration to support configurable number of endpoints, interfaces, alternate interfaces and configurations.
- LTTS USB 3.1 Host Controller can be configured to support any combinations of USB 3.1 interface speeds – SSP (10 Gbps), SS(5 Gbps), HS (480 Mbps), FS(12 Mbps) and LS(1.5 Mbps). Eg combinations are SSP & SS only, SSP & SS & HS only, SSP & SS & HS & FS only, SS Only, SS & HS Only, SS & HS & FS Only, HS & FS Only etc.
- LTTS USB 3.1 Host Controller has full support for all low power features of the USB Specification supporting Suspend and Remote Wakeup, USB 3.1 Low Power States – U1/U2/U3 and USB 2.0 Link Power Management states – L1, L2.
- LTTS USB Controllers have been Silicon Proven in wide range of products such as Graphics Controller, Flash Storage Controllers, SATA Bridges with support for Bulk Streaming, Embedded Hosts, Docking Stations, Mobile Application Processors, Smart TV, Hubs.

Compliance
- LTTS USB 3.1 Host Controller IP core is compliant with USB 3.1 specification, Revision 1.0 and all associated ECN's.
- LTTS USB 3.1 Host Controller IP core is compliant with USB2.0 specification Revision 2.0 and all associated ECN's.
- LTTS USB 3.1 Host Controller IP core is compliant with xHCI Specification for USB Rev 1.0

Configurability
- Support for managing configurable number of Device Slots and Physical Ports.
- Hardware configurable support for USB speeds – SSP/SS/HS/FS/LS.
- Hardware configurable support for different use cases:
  - Optional simple slave mode operation for initiating/completing USB transactions for an area optimized implementation.
  - Optional proprietary LTTS DMA engine for generating USB transactions and limiting software overhead.

Feature Rich
- Internal data path width: 32
- External data path width: 32 / 64 bits
- USB PHY Interface
  - HS/FS/LS : ULPI, 8/16 bits UTMI or Serial Mode
  - SS : 8/16/32-bit PIPE Interface
  - SSP : 32-bit PIPE Interface
- Efficient buffering scheme.
- Data path Interface: AHB/AXI
- Register Path Interface: AHB

Application Layer Features
- Implements configurable xHCI Engine with configurable number of device slots, interrupters, internal buffers, root hub ports, optional support for host initiated stream data movement
- Alternately slave mode access to initiate USB transactions.
- Configurable Buffer Sizes.
- Asynchronous clocking between User Logic and Core.
- AHB/AXI System Interface. Optionally a 3rd party PCIe-AXI/AHB Bridge

Protocol and Link Layer Features
- Supports Interrupt/Bulk/Isochronous/Control Transfers.
- Supports configurable number of interfaces, configurations, and alternate settings while operating in device mode.
- CRC checking and generation
- Supports Protocol Layer Error Handling.
- Provides prioritized scheduling for periodic endpoints.
- Separate round robin scheduling algorithm within Periodic and Non-periodic endpoints pipes.
- Supports PTM
- Optionally, implements support for multiple outstanding IN transactions directed to different endpoints.
- Implements Type 1 and 2 Buffers
- Supports LFPS Signaling, SCD/LBPM Messaging
- Option to enable/disable scrambling
- Supports Master and Slave Loopback mode for PHY layer testing
- Supports Compliance mode entry as per specification.
- Optional Support for Type C Connector Interface

Register Support
- Supports CSR, PL, PM registers for Device mode of operation.
- Simple slave interface to access these registers.
- Additional design specific debug, control and status registers.

Power Management Support
- Supports USB Suspend state and supports remote wakeup devices.
- Supports all SS/SSP Link Power Management States – U1, U2, U3
- Supports all HS/FS USB Link Power Management States – L1, L2.
- Supports system low power and related system states such as Sleep, Hibernate, Warm/ Cold boot etc.
- Support for clock gating and multi-power-well support.

L&TTS USB 3.0 OTG Controller

PRODUCT BRIEF

USB 3.0/3.1 SOLUTIONS

LTTS are pioneers in USB controller Solutions. LTTS provides highly configurable USB 3.0 OTG/Dual-Role Controller IP Core. Our Host, Device, Hub are Silicon Realized and also USB-IF certified by our customers. LTTS provides highly configurable and scalable USB 3.0 OTG/Dual-Role controller IP Core for wide range of applications.

With a strong focus and expertise in delivering engineering services, LTTS works closely with clients in understanding their requirements, providing optimized configuration of the IP Core to meet specific requirements and in addition customizing the IP core for clients product differentiation. Extended engineering service engagements enable clients to utilize LTTS core development team to be deployed for fail safe integration of the IP in the clients SoC/end-product. All licensees are also provided with validation platforms along with necessary firmware support which can be used to functionally validate the product prior to tape-out mitigating risks.

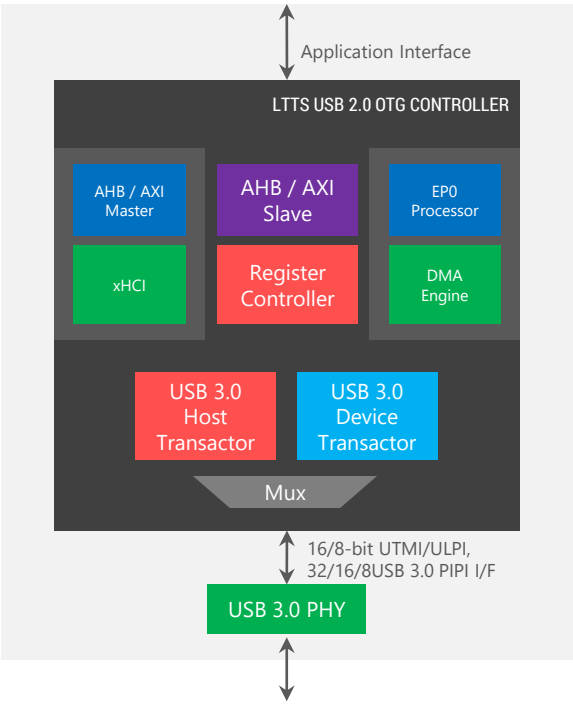
All IP's are provided as a complete solution consisting of a comprehensive verification suite, Clock Domain Crossing, Synthesis, and Logical equivalence constraints and waivers as applicable which are reusable at SoC level, along with pre-verified and interoperate proven with partner PHY solutions

LTTS USB 3.0 OTG controller are designed for compliance with USB2.0 specification Revision 2.0 and all associated ECN's and USB OTG EH 2 Revision 1.1a and all associated ECN's. While operating in Host mode, based on configuration selected, it is compliant with xHCI, enabling standard Windows, Linux, Android drivers to be reused minimizing software development overheads and associated risks involved with custom bare metal driver solutions. Its Physical interface is compliant with USB 3.0 Pipe Specification v4.3 (for SS mode) and ULPI+ or 8/16 bits UTMI PLUS Level3 specification (for HS/FS/LS mode). The system interface is compliant with either AHB and/or AXI interface allowing easy integration. Optional custom bridges can be bundled as a service offering. Additionally, while operating in host mode, LTTS USB 3.0 OTG controller can be configured to support either one device connected directly to its port, or multiple devices connected via hubs.

LTTS USB 3.0 OTG controller, while operating in device mode, can optionally include a LTTS proprietary high performance DMA engine for moving USB payloads. The register interface of the DMA Engine is very simple allowing device side class specific function drivers to be implemented easily. Reference mass storage class device side function drivers are made available to all licensees. The same high performance DMA engine can be reused optionally for host mode operation, in which case custom bare metal drivers can be developed to manage the connected devices allowing highly optimized footprint for hardware and software. All buffering associated with the DMA Engine are configurable based on latency and performance requirements.

LTTS USB 3.0 OTG controller while operating in device mode can optionally include a LTTS proprietary EP0 processor block for managing all Standard Requests directed to the control endpoint minimizing software development overhead. Class and Vendor specific requests directed to Control endpoint are routed via the DMA engine to software for processing.

Optionally, the controller can be provided with no DMA Engine and no buffering and operates in a cut-through mode forwarding and receiving USB payloads and managing only the USB protocol. Customer may in this case implement its own differentiated DMA Engine. Optionally, a simple transmit and receive buffer is included in this configuration which can be accessed by software over the slave register access interface which is typically AHB. This option results in very low footprint hardware which can be used in cases where the software can completely manage the USB traffic – including the sequencing of the USB transactions.



DESIGN ATTRIBUTES

- Highly modular and configurable design
- Layered architecture
- Fully synchronous design
- Supports both sync and async reset
- Clearly de-marked clock domains
- Extensive clock gating support
- Multiple Power Well Support
- Software control for key features

PRODUCT PACKAGE

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    - Verification Guide
    - Synthesis Guide
- FPGA Platform for Pre-Tape-out Validation
- Reference Firmware

FEATURES

- LTTS USB 3.0 OTG Controller can be configured to support all types of USB transfers – Bulk, Interrupt and Isochronous. While operating in Device Mode it can be dynamically configured to support configurable number of endpoints, interfaces, alternate interfaces and configurations.
- LTTS USB 3.0 OTG Controller can be configured to support any combinations of USB 3.0 interface speeds – LS(1.5 Mbps), FS (12.0 Mbps), HS (480 Mbps). Eg combinations are LS Only, FS Only, HS Only, LS and FS Only, FS and HS Only etc.
- LTTS USB 3.0 OTG Controller has full support for all low power features of the USB Specification supporting Suspend, Remote Wakeup and USB 3.0 Link Management States - U1, U2, U3 and USB 2.0 Link Power Management states – L1, L2.
- LTTS USB 3.0 OTG controller has full support for all USB 2.0 test modes features as well as USB 3.0 compliance and USB 3.0 loopback modes which is required for obtaining USB-IF certification.
- LTTS USB 3.0 OTG Controller has full support for OTG features such as RSP, SRP, HNP and ADP along with software configurable options to turn on/off these features.
- LTTS USB Controllers have been Silicon Proven in wide range of products such as Graphics Controller, Flash Storage Controllers, SATA Bridges with support for Bulk Streaming, Embedded Hosts, Docking Stations, Mobile Application Processors, Smart TV, Hubs.

Compliance
- LTTS USB OTG Controller IP core is compatible with USB3.0 specification Revision 2.0 and all associated ECN's.
- LTTS USB OTG Controller IP core is compatible with USB2.0 specification Revision 2.0 and all associated ECN's.
- LTTS USB OTG Controller IP core compatible with USB OTG EH 3.0 Revision 1.1 and all associated ECN's.
- LTTS USB OTG Controller IP core compatible with USB OTG EH 2 Revision 1.1a and all associated ECN's.
- LTTS USB OTG Controller IP core operating in host mode is optionally compliant with xHCI specification version 1.1.

Configurability
- Support for managing configurable number of endpoints for device mode.
- Hardware configurable support for all optional features – viz., RSP/SRP/ADP/HNP support
- Hardware configurable support for USB speeds – SS/HS/FS/LS.
- Hardware configurable support for different use cases:
  - Optional simple slave mode operation for initiating/completing USB transactions for an area optimized implementation. Can be used for both host and device mode.
  - Optional standard based DMA engine based on xHCI, while operating in host mode allowing standard drivers to be reused. For device mode uses LTTS proprietary DMA controller is used.
  - Optional proprietary LTTS DMA engine for initiating/completing USB transactions limiting software overhead. Can be used with Host and Device mode operation.

Feature Rich
- Internal data path width: 32/64 bits
- External data path width: 32 / 64 bits
- USB2 PHY Interface: ULPI, 8/16 bits UTMI PLUS Level3
- USB3 PHY Interface: USB 3.0 32/16/8-bit PIPE
- Efficient buffering scheme.
- DMA path Interface: AHB/AXI
- Register Path Interface: AHB

OTG Specific Features
- Implements Session Request Protocol
- Supports Host Negotiation Protocol Polling
- Supports Host Negotiation Protocol logic with software configurable option to enable/disable this feature
- Supports Role Swap Protocol.
- Supports OTG, OTG Device Notification registers

Application Layer Features
- Host Mode Support using any of the following :
  - SS, HS, FS and LS supported with a single Host controller based on xHCI Specification.
  - Optionally device mode DMA Controller reused for supporting SS/HS/FS/LS mode transfers in Host mode also.
  - Optionally, a simple slave mode access to trigger USB transaction.
- While operating device Mode,
  - An optional DMA Controller to move USB data payloads or
  - A simple slave mode access to trigger responses to USB transactions initiated by the Host.
  - An optional EP0 processor to autonomously process all standard requests initiated by the Host.

Protocol Layer Features
- Supports Interrupt/Bulk/Isochronous/Control Transfers.
- Supports SS Bulk Streaming Endpoints, and USB 2.0 High Bandwidth Interrupt and Isochronous endpoints.
- Supports configurable number of interfaces, configurations, and alternate settings while operating in device mode.
- Supports configurable endpoint characteristics – for Maximum Packet Size, Endpoint Type etc.
- CRC32 Checking and generation for SS Data and Header Packets.
- CRC16 checking and generation for HS/FS/LS data packets.
- CRC5 generation and checking for Tokens.
- Supports Split Transfers for FS/LS devices connected to HS Hubs while operating in Embedded Host Mode.
- Supports preamble for LS transfers while operating in Embedded Host Mode.
- Supports Protocol Layer Error Handling.
- Provides prioritized scheduling for periodic endpoints.
- Separate round robin scheduling algorithm within Periodic and Non-periodic endpoints pipes.

Root hub Features for Host Mode of Operation
- Supports USB 3.0 Link Power Management
- Support USB 2.0 LPM transactions.
- Supports USB 3.0 Loopack and Compliance Mode.
- Support USB 2.0 Test mode.
- Configurable number of Downstream ports for Embedded Host Applications.
- Supports multiple devices connected under SS/HS/FS hub for Embedded Host Applications.

Register Support
- Implements all the xHCI compliant registers.
- Supports CSR, Link, PL, PM registers for Device mode of operation.
- Simple slave interface to access these registers.
- Additional design specific debug, control and status registers.

Power Management Support
- Supports USB Suspend state and supports remote wakeup devices.
- Supports all HS/FS USB Link Power Management States – L1, L2.
- Supports all SS USB Link Power Management States – U1, U2, and U3.
- Supports system low power and related system states such as Sleep, Hibernate, Warm/ Cold boot etc.
- Support for clock gating and multi-power-well support.

L&TTS USB 3.1 Device Controller

PRODUCT BRIEF

USB 3.0/3.1 SOLUTIONS

LTTS are pioneers in USB controller Solutions. LTTS provides highly configurable and scalable USB 3.1 Host/Device/Dual-Mode controller IP Core for wide range of applications.

With a strong focus and expertise in delivering engineering services, LTTS works closely with clients in understanding their requirements, providing optimized configuration of the IP Core to meet specific requirements and in addition customizing the IP core for clients product differentiation. Extended engineering service engagements enable clients to utilize LTTS core development team to be deployed for fail safe integration of the IP in the clients SoC/end-product. All licensees are also provided with validation platforms along with necessary firmware support which can be used to functionally validate the product prior to tape-out mitigating risks.

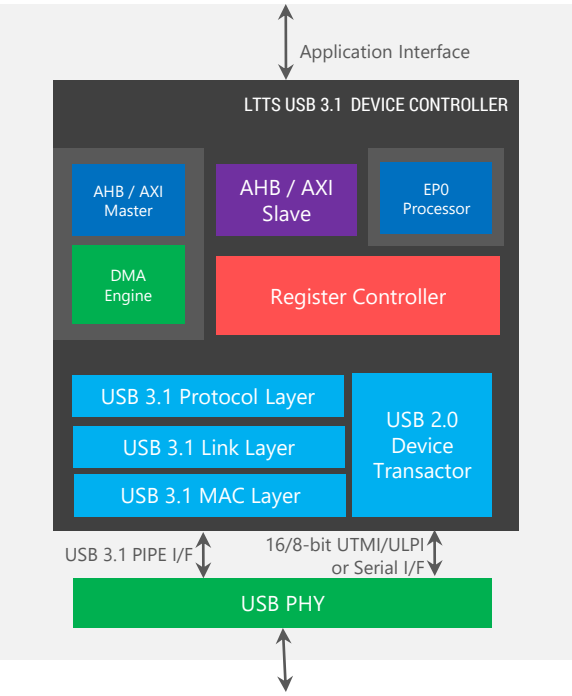
All IP's are provided as a complete solution consisting of a comprehensive verification suite, Clock Domain Crossing, Synthesis, and Logical equivalence constraints and waivers as applicable which are reusable at SoC level, along with pre-verified and interoperate proven with partner PHY solutions

LTTS USB 3.1 controller are designed for compliance with USB3.1 specification, Revision 1.0 and all associated ECN's, USB specifications Rev 2.0 and all associated ECN's.

LTTS USB 3.1 Device controller, can optionally include a LTTS proprietary high performance DMA engine for moving USB payloads. The register interface of the DMA Engine is very simple allowing device side class specific function drivers to be implemented easily. Reference mass storage class device side function drivers are made available to all licensees. All buffering associated with the DMA Engine are configurable based on latency and performance requirements.

LTTS USB 3.1 Device controller can optionally include a LTTS proprietary EP0 processor block for managing all Standard Requests directed to the control endpoint minimizing software development overhead. Class and Vendor specific requests directed to Control endpoint are routed via the DMA engine to software for processing.

Optionally, the controller can be provided with no DMA Engine and no buffering and operates in a cut-through mode forwarding and receiving USB payloads and managing only the USB protocol. Customer may in this case implement its own differentiated DMA Engine. Optionally, a simple transmit and receive buffer is included in this configuration which can be accessed by software over the slave register access interface which is typically AHB. This option results in very low footprint hardware which can be used in cases where the software can completely manage the USB traffic – including the sequencing of the USB transactions.



DESIGN ATTRIBUTES

- Highly modular and configurable design
- Layered architecture
- Fully synchronous design
- Supports both sync and async reset
- Clearly de-marked clock domains
- Extensive clock gating support
- Multiple Power Well Support
- Software control for key features

PRODUCT PACKAGE

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- Test cases
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- Documentation
    - Design Guide
    - Verification Guide
    - Synthesis Guide
- FPGA Platform for Pre-Tape-out Validation
- Reference Firmware

FEATURES

- LTTS USB 3.1 Device Controller can be configured to support all types of USB transfers – Bulk, Interrupt and Isochronous.
- Allows dynamic configuration to support configurable number of endpoints, interfaces, alternate interfaces and configurations.
- LTTS USB 3.1 Device Controller can be configured to support any combinations of USB 3.1 interface speeds – SSP (10 Gbps), SS(5 Gbps), HS (480 Mbps), FS(12 Mbps) and LS(1.5 Mbps). Eg combinations are SSP & SS only, SSP & SS & HS only, SSP & SS & HS & FS only, SS Only, SS & HS Only, SS & HS & FS Only.
- LTTS USB 3.1 Device Controller has full support for all low power features of the USB Specification supporting Suspend and Remote Wakeup, USB 3.1 Low Power States – U1/U2/U3 and USB 2.0 Link Power Management states – L1, L2.
- LTTS USB Controllers have been Silicon Proven in wide range of products such as Graphics Controller, Flash Storage Controllers, SATA Bridges with support for Bulk Streaming, Embedded Hosts, Docking Stations, Mobile Application Processors, Smart TV, Hubs.

Compliance
- LTTS USB 3.1 Device Controller IP core is compliant with USB 3.1 specification, Revision 1.0 and all associated ECN's.
- LTTS USB 3.1 Device Controller IP core is compliant with USB2.0 specification Revision 2.0 and all associated ECN's.

Configurability
- Support for managing configurable number of endpoints.
- Optional inclusion of EP0 processor for autonomous processing of standard requests
- Hardware configurable support for USB speeds – SSP/SS/HS/FS/LS.
- Hardware configurable support for different use cases:
  - Optional simple slave mode operation for initiating/completing USB transactions for an area optimized implementation.
  - Optional proprietary LTTS DMA engine for generating responses to USB transactions and limiting software overhead.

Feature Rich
- Internal data path width: 32
- External data path width: 32 / 64 bits
- USB PHY Interface
  - HS/FS/LS : ULPI, 8/16 bits UTMI or Serial Mode
  - SS : 8/16/32-bit PIPE Interface
  - SSP : 32-bit PIPE Interface
- Efficient buffering scheme.
- DMA path Interface: AHB/AXI
- Register Path Interface: AHB

Application Layer Features
- An optional DMA Controller to move USB data payloads or
- A simple slave mode access to trigger responses to USB transactions initiated by the Host.
- An optional EP0 processor to autonomously process all standard requests initiated by the Host.
- Asynchronous clocking between User Logic and Core.
- AHB/AXI System Interface

Protocol and Link Layer Features
- Supports Interrupt/Bulk/Isochronous/Control Transfers.
- Supports configurable number of interfaces, configurations, and alternate settings while operating in device mode.
- Supports configurable endpoint characteristics – for Maximum Packet Size, Endpoint Type etc.
- CRC checking and generation
- Supports Protocol Layer Error Handling.
- Provides prioritized scheduling for periodic endpoints.
- Separate round robin scheduling algorithm within Periodic and Non-periodic endpoints pipes.
- Supports PTM
- Implements support for multiple outstanding IN transactions directed to different endpoints.
- Implements Type 1 and 2 Buffers
- Supports LFPS Signaling, SCD/LBPM Messaging
- Option to enable/disable scrambling
- Supports Master and Slave Loopback mode for PHY layer testing
- Supports Compliance mode entry as per specification.
- Optional Support for Type C Connector Interface

Register Support
- Supports CSR, PL, PM registers for Device mode of operation.
- Simple slave interface to access these registers.
- Additional design specific debug, control and status registers.

Power Management Support
- Supports USB Suspend state and supports remote wakeup devices.
- Supports all SS/SSP Link Power Management States – U1, U2, U3
- Supports all HS/FS USB Link Power Management States – L1, L2.
- Supports system low power and related system states such as Sleep, Hibernate, Warm/ Cold boot etc.
- Support for clock gating and multi-power-well support.

L&T TS USB 2.0 Host Controller

PRODUCT BRIEF

LTTS are pioneers in USB controller Solutions. LTTS provides highly configurable and scalable USB 2.0 Host/Device/Dual-Mode controller IP Core for wide range of applications.

With a strong focus and expertise in delivering engineering services, LTTS works closely with clients in understanding their requirements, providing optimized configuration of the IP Core to meet specific requirements and in addition customizing the IP core for clients product differentiation. Extended engineering service engagements enable clients to utilize LTTS core development team to be deployed for fail safe integration of the IP in the clients SoC/end-product. All licensees are also provided with validation platforms along with necessary firmware support which can be used to functionally validate the product prior to tape-out mitigating risks.

All IP's are provided as a complete solution consisting of a comprehensive verification suite, Clock Domain Crossing, Synthesis, and Logical equivalence constraints and waivers as applicable which are reusable at SoC level, along with pre-verified and interoperate proven with partner PHY solutions

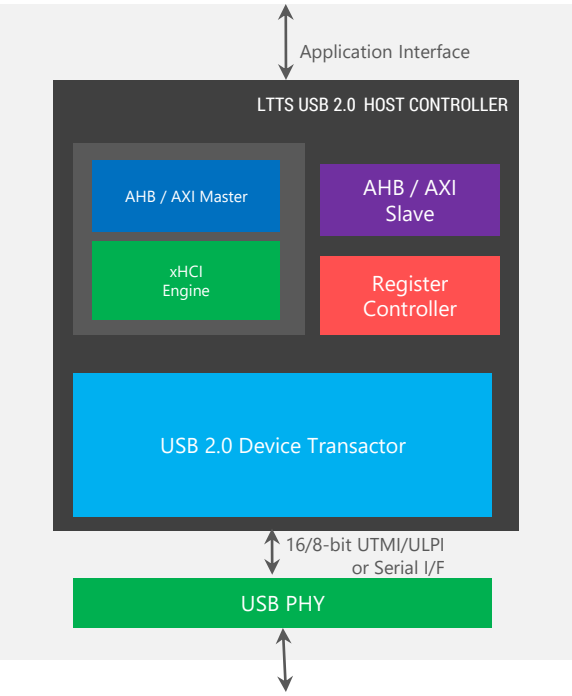
LTTS USB 2.0 controller are designed for compliance with USB2.0 specification, Revision 1.0 and all associated ECN's.

LTTS USB 2.0 Host controller is architected to optionally include a High Performance DMA Engine either based on xHCI Specification. All buffering associated with the DMA Engine are configurable based on latency and performance requirements. The core can be configured to support full fledged xHCI implementations for use in standard PCIe-USB bus adaptors/chip sets or be configured with a subset of features for embedded applications requiring limited host functionality.

LTTS USB 2.0 Host Controller based on xHCI specification can be used in systems using any OS which provides xHCI/USB Stacks such as – Android, Linux, Windows.

LTTS USB 2.0 Host controller exposes either a AXI or AHB Master Interface for the Datapath and an AHB Slave Interface for Register Access. Optionally, a interoperate proven 3rd Party PCIe-AXI/AHB bridge can be provided for use in standard desktop / server applications.

Optionally, the controller can be provided with no xHCI Engine and no buffering and operates in a cut-through mode forwarding and receiving USB payloads and managing only the USB protocol. Customer may in this case implement its own differentiated DMA Engine. Optionally, a simple transmit and receive buffer is included in this configuration which can be accessed by software over the slave register access interface which is typically AHB. This option results in very low footprint hardware which can be used in cases where the software can completely manage the USB traffic – including the sequencing of the USB transactions.



DESIGN ATTRIBUTES

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    - Synthesis Guide
- FPGA Platform for Pre-Tape-out Validation

FEATURES

- LTTS USB 2.0 Host Controller can be configured to support all types of USB transfers – Bulk, Interrupt and Isochronous.
- Allows dynamic configuration to support configurable number of endpoints, interfaces, alternate interfaces and configurations.
- LTTS USB 2.0 Host Controller can be configured to support any combinations of USB 2.0 interface speeds – HS (480 Mbps), FS(12 Mbps) and LS(1.5 Mbps). Eg combinations are HS, FS, and LS, HS & FS only, FS & LS only, HS only, FS only etc.
- LTTS USB 2.0 Host Controller has full support for all low power features of the USB Specification supporting Suspend and Remote Wakeup and USB 2.0 Link Power Management states – L1, L2.
- LTTS USB Controllers have been Silicon Proven in wide range of products such as Graphics Controller, Flash Storage Controllers, SATA Bridges with support for Bulk Streaming, Embedded Hosts, Docking Stations, Mobile Application Processors, Smart TV, Hubs.

Compliance
- LTTS USB 2.0 Host Controller IP core is compliant with USB2.0 specification Revision 2.0 and all associated ECN's.
- LTTS USB 2.0 Host Controller IP core is compliant with xHCI Specification for USB Rev 1.1

Configurability
- Support for hardware configurable number of device slots.
- Hardware configurable support for USB speeds –HS/FS/LS.
- Hardware configurable support for different use cases:
  - Optional simple slave mode operation for initiating/completing USB transactions for an area optimized implementation.
  - Optional proprietary LTTS DMA engine for generating USB transactions and limiting software overhead.

Feature Rich
- Internal data path width: 32
- External data path width: 32 / 64 bits
- USB PHY Interface
  - HS/FS/LS : ULPI, 8/16 bits UTMI or Serial Mode
- Efficient buffering scheme.
- Data path Interface: AHB/AXI
- Register Path Interface: AHB

Application Layer Features
- Implements configurable xHCI Engine with configurable number of device slots, interrupters, internal buffers, root hub ports, optional support for host initiated stream data movement
- Alternately slave mode access to initiate USB transactions.
- Configurable Buffer Sizes.
- Asynchronous clocking between User Logic and Core.
- AHB/AXI System Interface. Optionally a 3rd party PCIe-AXI/AHB Bridge

Protocol Layer Features
- Supports Interrupt/Bulk/Isochronous/Control Transfers.
- CRC16 checking and generation for HS/FS/LS data packets.
- CRC5 generation and checking for Tokens.
- Supports Split Transfers for FS/LS devices connected to HS Hubs while operating in Embedded Host Mode.
- Supports preamble for LS transfers while operating in Embedded Host Mode.
- Supports Protocol Layer Error Handling.
- Provides prioritized scheduling for periodic endpoints.
- Separate round robin scheduling algorithm within Periodic and Non-periodic endpoints pipes.
- Optional Support for Type C Connector Interface

Register Support
- Supports CSR, PL, PM registers for Device mode of operation.
- Simple slave interface to access these registers.
- Additional design specific debug, control and status registers.

Power Management Support
- Supports USB Suspend state and supports remote wakeup devices.
- Supports all HS/FS USB Link Power Management States – L1, L2.
- Supports system low power and related system states such as Sleep, Hibernate, Warm/ Cold boot etc.
- Support for clock gating and multi-power-well support.

L&TTS USB 2.0 OTG Controller

PRODUCT BRIEF

LTTS are pioneers in USB controller Solutions. LTTS provides highly configurable USB 2.0 OTG/Dual-Role Controller IP Core. Our Host, Device, Hub are Silicon Realized and also USB-IF certified by our customers. LTTS provides highly configurable and scalable USB 2.0 OTG/Dual-Role controller IP Core for wide range of applications.

With a strong focus and expertise in delivering engineering services, LTTS works closely with clients in understanding their requirements, providing optimized configuration of the IP Core to meet specific requirements and in addition customizing the IP core for clients product differentiation. Extended engineering service engagements enable clients to utilize LTTS core development team to be deployed for fail safe integration of the IP in the clients SoC/end-product. All licensees are also provided with validation platforms along with necessary firmware support which can be used to functionally validate the product prior to tape-out mitigating risks.

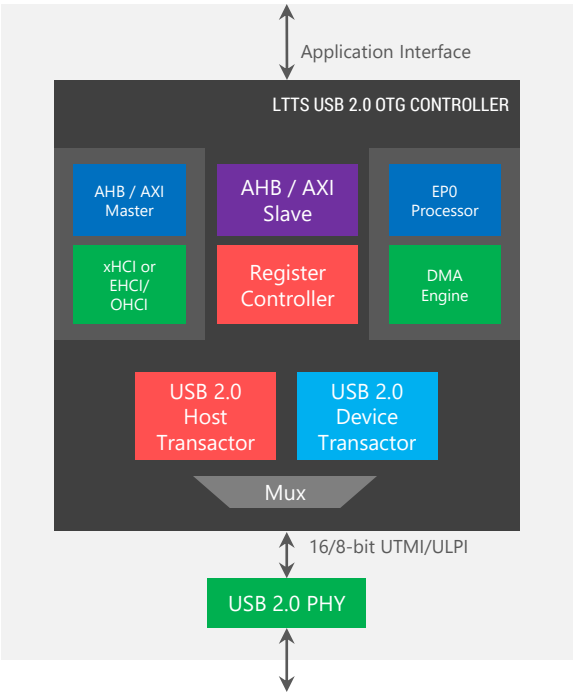
All IP's are provided as a complete solution consisting of a comprehensive verification suite, Clock Domain Crossing, Synthesis, and Logical equivalence constraints and waivers as applicable which are reusable at SoC level, along with pre-verified and interoperate proven with partner PHY solutions

LTTS USB 2.0 OTG controller are designed for compliance with USB2.0 specification Revision 2.0 and all associated ECN's and USB OTG EH 2 Revision 1.1a and all associated ECN's. While operating in Host mode, based on configuration selected, optionally, it is compliant with either xHCI, EHCI/OHCI enabling standard Windows, Linux, Android drivers to be reused minimizing software development overheads and associated risks involved with custom bare metal driver solutions. Its Physical interface is compliant with either ULPI+ or 8/16 bits UTMI PLUS Level3 specification. The system interface is compliant with either AHB and/or AXI interface allowing easy integration. Optional custom bridges can be bundled as a service offering. Additionally, while operating in host mode, LTTS USB 2.0 OTG controller can be configured to support either one device connected directly to its port, or multiple devices connected via hubs.

LTTS USB 2.0 OTG controller, while operating in device mode, can optionally include a LTTS proprietary high performance DMA engine for moving USB payloads. The register interface of the DMA Engine is very simple allowing device side class specific function drivers to be implemented easily. Reference mass storage class device side function drivers are made available to all licensees. The same high performance DMA engine can be reused optionally for host mode operation, in which case custom bare metal drivers can be developed to manage the connected devices allowing highly optimized footprint for hardware and software. All buffering associated with the DMA Engine are configurable based on latency and performance requirements.

LTTS USB 2.0 OTG controller while operating in device mode can optionally include a LTTS proprietary EP0 processor block for managing all Standard Requests directed to the control endpoint minimizing software development overhead. Class and Vendor specific requests directed to Control endpoint are routed via the DMA engine to software for processing.

Optionally, the controller can be provided with no DMA Engine and no buffering and operates in a cut-through mode forwarding and receiving USB payloads and managing only the USB protocol. Customer may in this case implement its own differentiated DMA Engine. Optionally, a simple transmit and receive buffer is included in this configuration which can be accessed by software over the slave register access interface which is typically AHB. This option results in very low footprint hardware which can be used in cases where the software can completely manage the USB traffic – including the sequencing of the USB transactions.



DESIGN ATTRIBUTES

- Highly modular and configurable design
- Layered architecture
- Fully synchronous design
- Supports both sync and async reset
- Clearly de-marked clock domains
- Extensive clock gating support
- Multiple Power Well Support
- Software control for key features

PRODUCT PACKAGE

- Configurable RTL Code
- HDL based test bench and behavioral models
- Test cases
- Protocol checkers, bus watchers and performance monitors
- Configurable synthesis shell
- Documentation
    - Design Guide
    - Verification Guide
    - Synthesis Guide
- FPGA Platform for Pre-Tape-out Validation
- Reference Firmware

FEATURES

- LTTS USB 2.0 OTG Controller can be configured to support all types of USB transfers – Bulk, Interrupt and Isochronous. While operating in Device Mode it can be dynamically configured to support configurable number of endpoints, interfaces, alternate interfaces and configurations.
- LTTS USB 2.0 OTG Controller can be configured to support any combinations of USB 2.0 interface speeds – LS(1.5 Mbps), FS (12.0 Mbps), HS (480 Mbps). Eg combinations are LS Only, FS Only, HS Only, LS and FS Only, FS and HS Only etc.
- LTTS USB 2.0 OTG Controller has full support for all low power features of the USB Specification supporting Suspend, Remote Wakeup and Link Power Management states – L1, L2.
- LTTS USB 2.0 OTG controller has full support for all test modes features which is required for obtaining USB-IF certification.
- LTTS USB 2.0 OTG Controller has full support for OTG features such as SRP, HNP and ADP along with software configurable options to turn on/off these features.
- LTTS USB Controllers have been Silicon Proven in wide range of products such as Graphics Controller, Flash Storage Controllers, SATA Bridges with support for Bulk Streaming, Embedded Hosts, Docking Stations, Mobile Application Processors, Smart TV, Hubs.

Compliance
- LTTS USB OTG Controller IP core is compatible with USB2.0 specification Revision 2.0 and all associated ECN's.
- LTTS USB OTG Controller IP core with USB OTG EH 2 Revision 1.1a and all associated ECN's.
- LTTS USB OTG Controller IP core operating in host mode is optionally compliant with xHCI specification version 1.1.
- LTTS USB OTG Controller IP core operating in host mode is optionally compliant with EHCI specification version 1.0
- LTTS USB OTG Controller IP core operating in host mode is optionally compliant with OHCI specification version 1.0a.

Configurability
- Support for managing configurable number of endpoints for device mode.
- Hardware configurable support for all optional features – viz., SRP/RSP/HNP support
- Hardware configurable support for USB speeds – HS/FS/LS.
- Hardware configurable support for different use cases:
  - Optional simple slave mode operation for initiating/completing USB transactions for an area optimized implementation. Can be used for both host and device mode.
  - Optional standard based DMA engine based on either xHCI, EHCI, OHCI while operating in host mode allowing standard drivers to be reused. For device mode uses LTTS proprietary DMA controller is used.
  - Optional proprietary LTTS DMA engine for initiating/completing USB transactions limiting software overhead. Can be used with Host and Device mode operation.

Feature Rich
- Internal data path width: 32/64 bits
- External data path width: 32 / 64 bits
- USB2 PHY Interface: ULPI, 8/16 bits UTMI PLUS Level3
- Efficient buffering scheme.
- DMA path Interface: AHB/AXI
- Register Path Interface: AHB

OTG Specific Features
- Implements Session Request Protocol
- Supports Host Negotiation Protocol Polling
- Supports Host Negotiation Protocol logic with software configurable option to enable/disable this feature
- Supports OTG, OTG Device Notification registers

Application Layer Features
- Host Mode Support using any of the following :
  - HS, FS and LS supported with a single Host controller based on xHCI Specification.
  - Companion controller model – HS Mode supported based on EHCI Specification and FS/LS Mode support using OHCI specification.
  - Optionally device mode DMA Controller reused for supporting HS/FS/LS mode transfers in Host mode also.
  - Optionally, a simple slave mode access to trigger USB transaction.
- While operating device Mode,
  - An optional DMA Controller to move USB data payloads or
  - A simple slave mode access to trigger responses to USB transactions initiated by the Host.
  - An optional EP0 processor to autonomously process all standard requests initiated by the Host.

Protocol Layer Features
- Supports Interrupt/Bulk/Isochronous/Control Transfers.
- Supports High Bandwidth Interrupt and Isochronous endpoints.
- Supports configurable number of interfaces, configurations, and alternate settings while operating in device mode.
- Supports configurable endpoint characteristics – for Maximum Packet Size, Endpoint Type etc.
- CRC16 checking and generation for HS/FS/LS data packets.
- CRC5 generation and checking for Tokens.
- Supports Split Transfers for FS/LS devices connected to HS Hubs while operating in Embedded Host Mode.
- Supports preamble for LS transfers while operating in Embedded Host Mode.
- Supports Protocol Layer Error Handling.
- Provides prioritized scheduling for periodic endpoints.
- Separate round robin scheduling algorithm within Periodic and Non-periodic endpoints pipes.

Root hub Features for Host Mode of Operation
- Support LPM transactions.
- Support USB 2.0 Test mode.
- Configurable number of Downstream ports for Embedded Host Applications.
- Supports multiple devices connected under HS/FS hub for Embedded Host Applications.

Register Support
- Implements all the xHCI (or OHCI/EHCI) compliant registers.
- Supports CSR, Link, PL, PM registers for Device mode of operation.
- Simple slave interface to access these registers.
- Additional design specific debug, control and status registers.

Power Management Support
- Supports USB Suspend state and supports remote wakeup devices.
- Supports all HS/FS USB Link Power Management States – L1, L2.
- Supports system low power and related system states such as Sleep, Hibernate, Warm/ Cold boot etc.
- Support for clock gating and multi-power-well support.

L&TTS USB 2.0 Device Controller

PRODUCT BRIEF

LTTS are pioneers in USB controller Solutions. LTTS provides highly configurable USB 2.0 Device Controller IP Core. Our Host, Device, Hub are Silicon Realized and also USB-IF certified by our customers. LTTS provides highly configurable and scalable USB 2.0 Device controller IP Core for wide range of applications.

With a strong focus and expertise in delivering engineering services, LTTS works closely with clients in understanding their requirements, providing optimized configuration of the IP Core to meet specific requirements and in addition customizing the IP core for clients product differentiation. Extended engineering service engagements enable clients to utilize LTTS core development team to be deployed for fail safe integration of the IP in the clients SoC/end-product. All licensees are also provided with validation platforms along with necessary firmware support which can be used to functionally validate the product prior to tape-out mitigating risks.

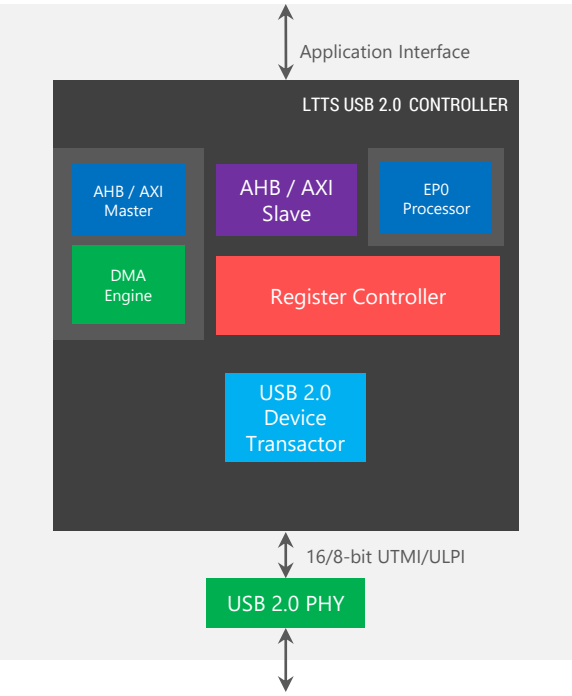
All IP's are provided as a complete solution consisting of a comprehensive verification suite, Clock Domain Crossing, Synthesis, and Logical equivalence constraints and waivers as applicable which are reusable at SoC level, along with pre-verified and interoperate proven with partner PHY solutions

LTTS USB 2.0 Device controller is designed for compliance with USB2.0 specification Revision 2.0 and all associated ECN's. Its Physical interface is compliant with either ULPI+ or 8/16 bits UTMI PLUS Level3 specification. The system interface is compliant with either AHB and/or AXI interface allowing easy integration. Optional custom bridges can be bundled as a service offering.

LTTS USB 2.0 Device controller can optionally include a LTTS proprietary high performance DMA engine for moving USB payloads. The register interface of the DMA Engine is very simple allowing device side class specific function drivers to be implemented easily. Reference mass storage class device side function drivers are made available to all licensees. All buffering associated with the DMA Engine are configurable based on latency and performance requirements.

LTTS USB Device controller can optionally include a LTTS proprietary EP0 processor block for managing all Standard Requests directed to the control endpoint minimizing software development overhead. Class and Vendor specific requests directed to Control endpoint are routed via the DMA engine to software for processing.

Optionally, the controller can be provided with no DMA Engine and no buffering and operates in a cut-through mode forwarding and receiving USB payloads and managing only the USB protocol. Customer may in this case implement its own differentiated DMA Engine. Optionally, a simple transmit and receive buffer is included in this configuration which can be accessed by software over the slave register access interface which is typically AHB. This option results in very low footprint hardware which can be used in cases where the software can completely manage the USB traffic – including the sequencing of the USB transactions.



DESIGN ATTRIBUTES

- Highly modular and configurable design
- Layered architecture
- Fully synchronous design
- Supports both sync and async reset
- Clearly de-marked clock domains
- Extensive clock gating support
- Multiple Power Well Support
- Software control for key features

PRODUCT PACKAGE

- Configurable RTL Code
- HDL based test bench and behavioral models
- Test cases
- Protocol checkers, bus watchers and performance monitors
- Configurable synthesis shell
- Documentation
    - Design Guide
    - Verification Guide
    - Synthesis Guide
- FPGA Platform for Pre-Tape-out Validation
- Reference Firmware

FEATURES

- LTTS USB 2.0 Device Controller can be configured to support all types of USB transfers – Bulk, Interrupt and Isochronous. While operating in Device Mode it can be dynamically configured to support configurable number of endpoints, interfaces, alternate interfaces and configurations.
- LTTS USB 2.0 Device Controller can be configured to support any combinations of USB 2.0 interface speeds – LS(1.5 Mbps), FS (12.0 Mbps), HS (480 Mbps). Eg combinations are LS Only, FS Only, HS Only, LS and FS Only, FS and HS Only etc.
- LTTS USB 2.0 Device Controller has full support for all low power features of the USB Specification supporting Suspend, Remote Wakeup and Link Power Management states – L1, L2.
- LTTS USB 2.0 Device controller has full support for all test modes features which is required for obtaining USB-IF certification.
- LTTS USB 2.0 Device Controller core is a USB-IF certified core.
- LTTS USB Controllers have been Silicon Proven in wide range of products such as Graphics Controller, Flash Storage Controllers, SATA Bridges with support for Bulk Streaming, Embedded Hosts, Docking Stations, Mobile Application Processors, Smart TV, Hubs.

Compliance
- LTTS USB Device Controller IP core is compatible with USB2.0 specification Revision 2.0 and all associated ECN's.

Configurability
- Support for managing configurable number of endpoints.
- Hardware configurable support for USB speeds – HS/FS/LS.
- Hardware configurable support for different use cases:
  - Optional simple slave mode operation for initiating/completing USB transactions for an area optimized implementation.
  - Optional proprietary LTTS DMA engine for initiating/completing USB transactions limiting software overhead.

Feature Rich
- Internal data path width: 32/64 bits
- External data path width: 32 / 64 bits
- USB2 PHY Interface: ULPI, 8/16 bits UTMI PLUS Level3
- Efficient buffering scheme.
- Data path Interface: AHB/AXI
- Register Path Interface: AHB

Application Layer Features
- An optional DMA Controller to move USB data payloads or
- A simple slave mode access to trigger responses to USB transactions initiated by the Host.
- An optional EP0 processor to autonomously process all standard requests initiated by the Host.

Protocol Layer Features
- Supports Interrupt/Bulk/Isochronous/Control Transfers.
- Supports High Bandwidth Interrupt and Isochronous endpoints.
- Supports configurable number of interfaces, configurations, and alternate settings while operating in device mode.
- Supports configurable endpoint characteristics – for Maximum Packet Size, Endpoint Type etc.
- CRC16 checking and generation for HS/FS/LS data packets.
- CRC5 generation and checking for Tokens.
- Supports preamble for LS transfers while operating in Embedded Host Mode.
- Supports Protocol Layer Error Handling.
- Provides prioritized scheduling for periodic endpoints.
- Separate round robin scheduling algorithm within Periodic and Non-periodic endpoints pipes.

Register Support
- Supports CSR, Link, PL, PM registers for Device mode of operation.
- Simple slave interface to access these registers.
- Additional design specific debug, control and status registers.

Power Management Support
- Supports USB Suspend state and supports remote wakeup devices.
- Supports all HS/FS USB Link Power Management States – L1, L2.
- Supports system low power and related system states such as Sleep, Hibernate, Warm/ Cold boot etc.
- Support for clock gating and multi-power-well support.

L&TTS USB 1.1 Device Controller

PRODUCT BRIEF

USB 1.1 SOLUTIONS

LTTS are pioneers in USB controller Solutions. LTTS provides highly configurable USB 1.1 Controller IP Core. LTTS provides highly configurable and scalable USB 1.1 Host/Device/Dual-Mode controller IP Core for wide range of applications.

With a strong focus and expertise in delivering engineering services, LTTS works closely with clients in understanding their requirements, providing optimized configuration of the IP Core to meet specific requirements and in addition customizing the IP core for clients product differentiation. Extended engineering service engagements enable clients to utilize LTTS core development team to be deployed for fail safe integration of the IP in the clients SoC/end-product. All licensees are also provided with validation platforms along with necessary firmware support which can be used to functionally validate the product prior to tape-out mitigating risks.

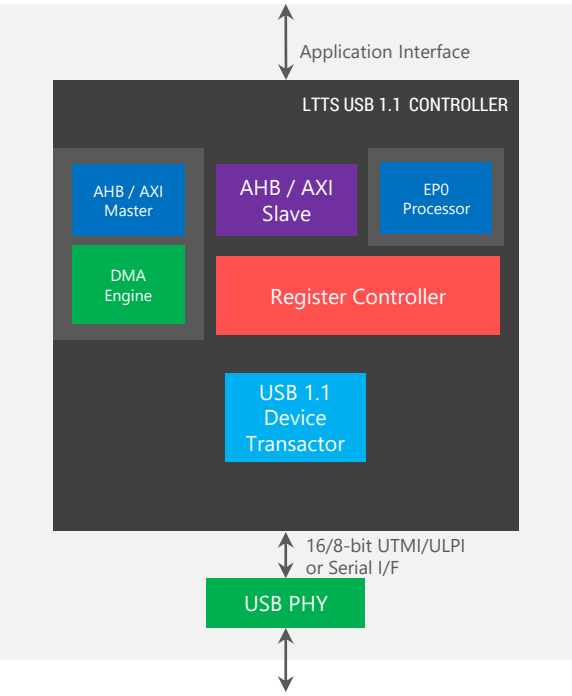
All IP's are provided as a complete solution consisting of a comprehensive verification suite, Clock Domain Crossing, Synthesis, and Logical equivalence constraints and waivers as applicable which are reusable at SoC level, along with pre-verified and interoperate proven with partner PHY solutions

LTTS USB 1.1 controller are designed for compliance with USB2.0 specification Revision 2.0 and all associated ECN's.

LTTS USB 1.1 Device controller, can optionally include a LTTS proprietary high performance DMA engine for moving USB payloads. The register interface of the DMA Engine is very simple allowing device side class specific function drivers to be implemented easily. Reference mass storage class device side function drivers are made available to all licensees. All buffering associated with the DMA Engine are configurable based on latency and performance requirements.

LTTS USB 1.1 Device controller can optionally include a LTTS proprietary EP0 processor block for managing all Standard Requests directed to the control endpoint minimizing software development overhead. Class and Vendor specific requests directed to Control endpoint are routed via the DMA engine to software for processing.

Optionally, the controller can be provided with no DMA Engine and no buffering and operates in a cut-through mode forwarding and receiving USB payloads and managing only the USB protocol. Customer may in this case implement its own differentiated DMA Engine. Optionally, a simple transmit and receive buffer is included in this configuration which can be accessed by software over the slave register access interface which is typically AHB. This option results in very low footprint hardware which can be used in cases where the software can completely manage the USB traffic – including the sequencing of the USB transactions.



DESIGN ATTRIBUTES

- Highly modular and configurable design
- Layered architecture
- Fully synchronous design
- Supports both sync and async reset
- Clearly de-marked clock domains
- Extensive clock gating support
- Multiple Power Well Support
- Software control for key features

PRODUCT PACKAGE

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    - Synthesis Guide
- FPGA Platform for Pre-Tape-out Validation
- Reference Firmware

FEATURES

- LTTS USB 1.1 Device Controller can be configured to support all types of USB transfers – Bulk, Interrupt and Isochronous.
- Allows dynamic configuration to support configurable number of endpoints, interfaces, alternate interfaces and configurations.
- LTTS USB 1.1 Device Controller can be configured to support any combinations of USB 1.1 interface speeds – LS(1.5 Mbps), FS (12.0 Mbps). Eg combinations are LS Only, FS Only, LS and FS Only.
- LTTS USB 1.1 Device Controller has full support for all low power features of the USB Specification supporting Suspend and Remote Wakeup and Link Power Management states – L1, L2.
- LTTS USB Controllers have been Silicon Proven in wide range of products such as Graphics Controller, Flash Storage Controllers, SATA Bridges with support for Bulk Streaming, Embedded Hosts, Docking Stations, Mobile Application Processors, Smart TV, Hubs.

Compliance
- LTTS USB 1.1 Device Controller IP core is compatible with USB2.0 specification Revision 2.0 and all associated ECN's.

Configurability
- Support for managing configurable number of endpoints.
- Optional inclusion of EP0 processor for autonomous processing of standard requests
- Hardware configurable support for USB speeds – FS/LS.
- Hardware configurable support for different use cases:
  - Optional simple slave mode operation for initiating/completing USB transactions for an area optimized implementation.
  - Optional proprietary LTTS DMA engine for generating responses to USB transactions and limiting software overhead.

Feature Rich
- Internal data path width: 32
- External data path width: 32 / 64 bits
- USB PHY Interface: ULPI, 8/16 bits UTMI or Serial Mode
- Efficient buffering scheme.
- DMA path Interface: AHB/AXI
- Register Path Interface: AHB

Application Layer Features
- An optional DMA Controller to move USB data payloads or
- A simple slave mode access to trigger responses to USB transactions initiated by the Host.
- An optional EP0 processor to autonomously process all standard requests initiated by the Host.

Protocol Layer Features
- Supports Interrupt/Bulk/Isochronous/Control Transfers.
- Supports configurable number of interfaces, configurations, and alternate settings while operating in device mode.
- Supports configurable endpoint characteristics – for Maximum Packet Size, Endpoint Type etc.
- CRC16 checking and generation for FS/LS data packets.
- CRC5 generation and checking for Tokens.
- Supports preamble for LS transfers while operating in Host Mode.
- Supports Protocol Layer Error Handling.
- Provides prioritized scheduling for periodic endpoints.
- Separate round robin scheduling algorithm within Periodic and Non-periodic endpoints pipes.

Register Support
- Supports CSR, PL, PM registers for Device mode of operation.
- Simple slave interface to access these registers.
- Additional design specific debug, control and status registers.

Power Management Support
- Supports USB Suspend state and supports remote wakeup devices.
- Supports all FS USB Link Power Management States – L1, L2.
- Supports system low power and related system states such as Sleep, Hibernate, Warm/ Cold boot etc.
- Support for clock gating and multi-power-well support.

IP & IP Enabled Services

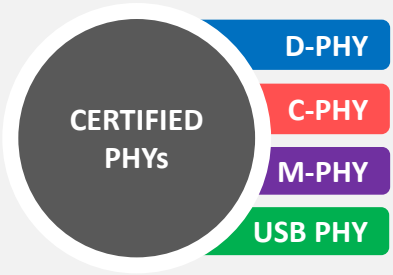
- Storage, Display, Imaging, Interconnect IPs
- Firmware and Application Software
- Platform Design

IC Design Services

Turnkey SoC Designs	RTL to GDS-II
Proof-of-Concept	Physical Design
Modeling	Silicon Validation
Design & Verification	IP Customization

Product Design

Application, Firmware and Diagnostic SW Development	Reference Design
Fast turnaround Board Design & Manufacturing	Full Product Design and Certification



FAST TURNAROUND EMERGING PROTOCOLS

VAST DOMAIN EXPERTISE

MIPI LEADER

AGILE & SCALABLE

ABOUT L&T TECHNOLOGY SERVICES

L&T Technology Services (formerly GDA Technologies) offers ASIC IPs, Total System Solutions for those IPs including Platform, Software and Driver, and also provide ASIC/FPGA/Platform/Software Design services. LTTS specialize in large high speed designs that require technological excellence and is an earlier adopter of multiple products. LTTS's proven services offer cost effective solution from concept to prototype, be it a system, ASIC/FPGA or Synthesizable IPs. We add value to customer design team with our strong technical skills in multiple domains, architecture, methodology, design and implementation skills. Our established relationships with mixed signal partners and silicon vendors ensure fast turnaround time for our designs.

L&T Technology Services is a Strategic Business Unit of L&T operating in diverse industry segments such as Aerospace, Automotive, Consumer Electronics, Consumer Packaged Goods, Marine, Power, Industrial Products, Oil and Gas, Medical Devices Telecom and Trucks & Off-Highway. It offers services in Embedded System, Mechanical and Civil Engineering, Product Life Cycle Management and Plant Engineering.

ABOUT L&T

Larsen & Toubro Limited (L&T) is a technology, engineering, construction, and manufacturing company. With revenue of USB 15bn, it is one of the largest and most respected companies in India's private sector. More than seven decades of a strong, customer-focused approach and the continuous quest for world-class quality have enabled it to attain and sustain leadership in all its major lines of business.

A WHOLLY-OWNED SUBSIDIARY OF **LARSEN & TOUBRO**

A "Top 5 Indian Player" in the ER&D space

Membership of professional bodies, key alliances and partnerships

170+ Global Customers

80 % of Business from EXISTING CLIENTS

42 Customers are Fortune 500 companies

9500+ employees across the globe

160+ Patents co-authored with clients

~30 % Year-on-year Growth rate

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